

ADS821

SpeedPLUS™ 10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW POWER: 380mW
- HIGH SNR: 58dB
- INTERNAL TRACK/HOLD
- PACKAGE: 28-Pin SOIC and SSOP

APPLICATIONS

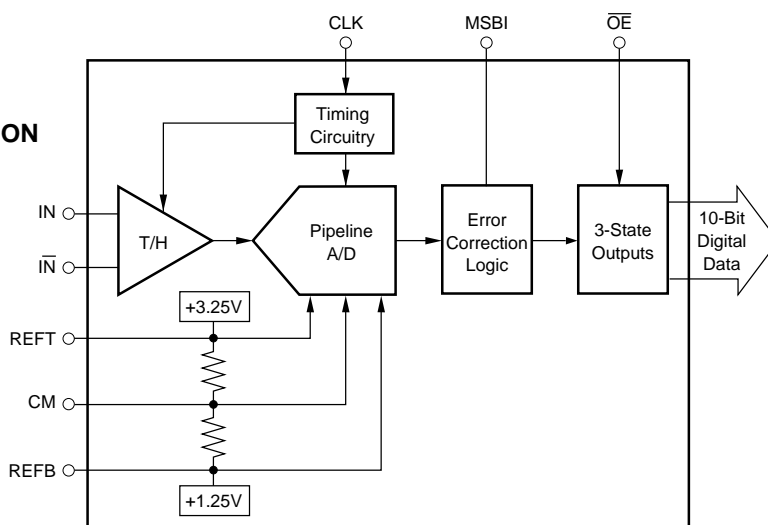
- VIDEO DIGITIZING
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- SET-TOP BOXES
- CABLE MODEMS
- CCD IMAGING
 - Color Copiers
 - Scanners
 - Camcorders
 - Security Cameras
 - Fax Machines
- IF AND BASEBAND DIGITIZATION
- TEST INSTRUMENTATION

DESCRIPTION

The ADS821 is a low power, monolithic 10-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS821 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 40MHz sampling rate. The ADS821 is available in 28-pin SOIC and SSOP packages.



SPECIFICATIONS (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U (SOIC)			ADS821E (SSOP)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUTS Logic Family Logic Coding Logic Levels	Logic Selectable Logic "LO", $C_L = 15\text{pF max}$ Logic "HI", $C_L = 15\text{pF max}$	Full	TTL/HCT Compatible CMOS SOB or BTC			TTL/HCT Compatible CMOS SOB or BTC			V
		Full	0		0.4	*		*	V
		Full	+2.5		$+V_S$	*		*	V
		Full		20	40		*	*	ns
3-State Enable Time				2				ns	
3-State Disable Time				2				ns	
POWER SUPPLY REQUIREMENTS									
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5	+5.25	*	*	*	V
Supply Current: $+I_S$	Operating	+25°C		76	88	*	*	*	mA
	Operating	Full		78	90	*	*	*	mA
Power Consumption	Operating	+25°C		380	440	*	*	*	mW
	Operating	Full		390	450	*	*	*	mW
Thermal Resistance, θ_{JA}				75		*	50	*	$^\circ\text{C/W}$

* Specifications same as ADS821U.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to $(+V_S + 300\text{mV})$
Logic Input	0V to $(+V_S + 300\text{mV})$
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V max
External Bottom Reference Voltage (REFB)	+1.1V min

NOTE: Stresses above these ratings may permanently damage the device.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
ADS821U	28-Pin SOIC	217	-40°C to +85°C
ADS821E	28-Pin SSOP	324	-40°C to +85°C

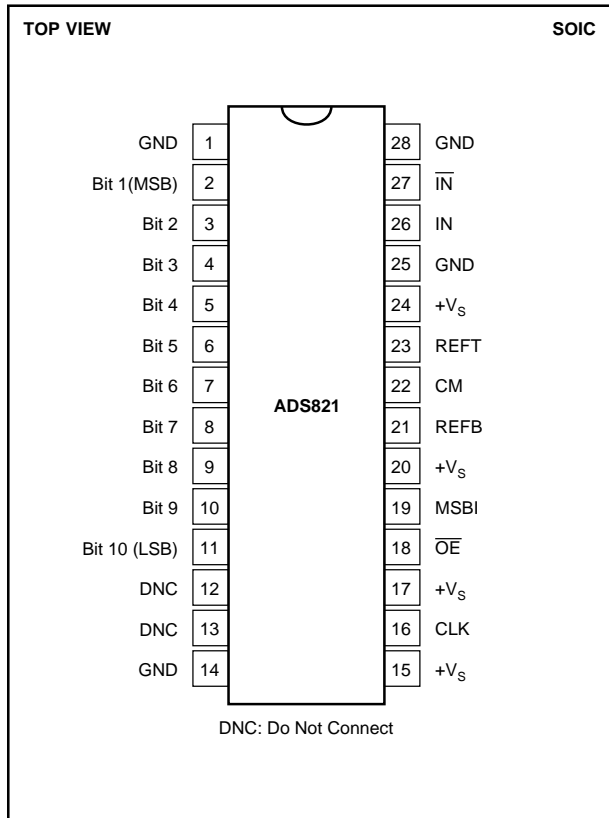
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

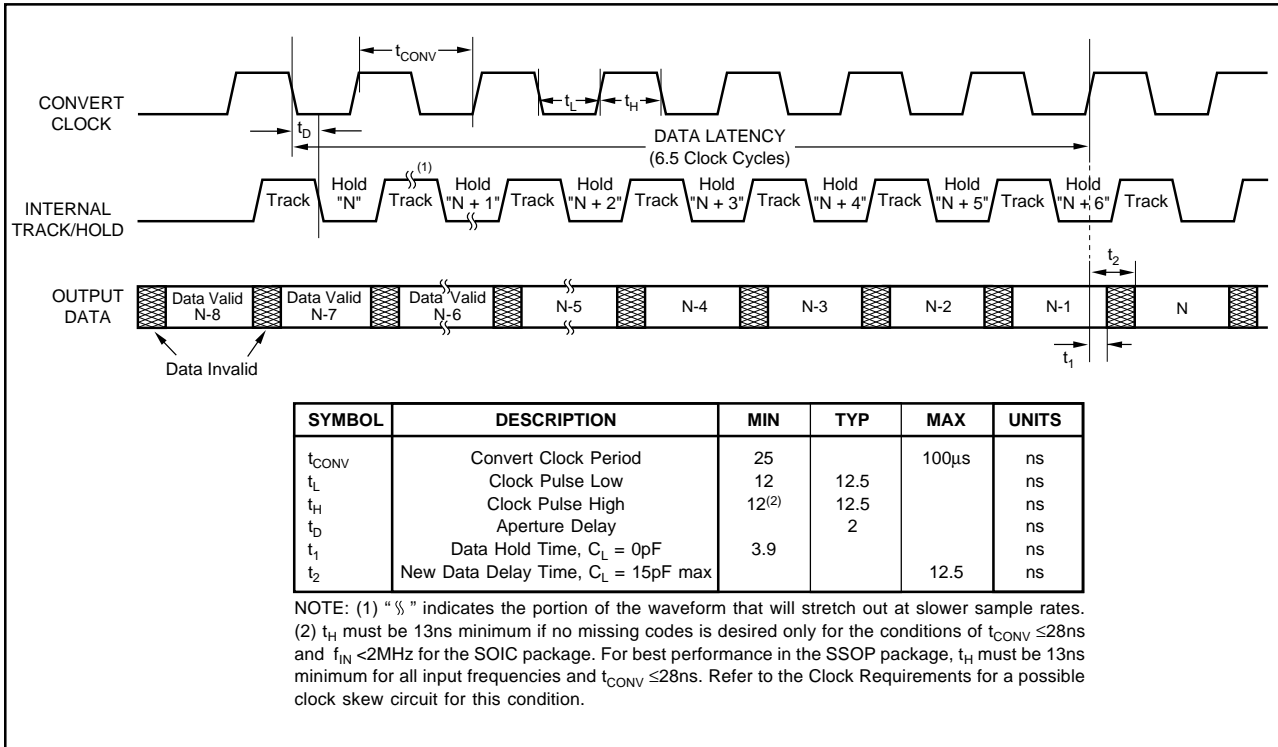
PIN CONFIGURATION



PIN DESCRIPTIONS

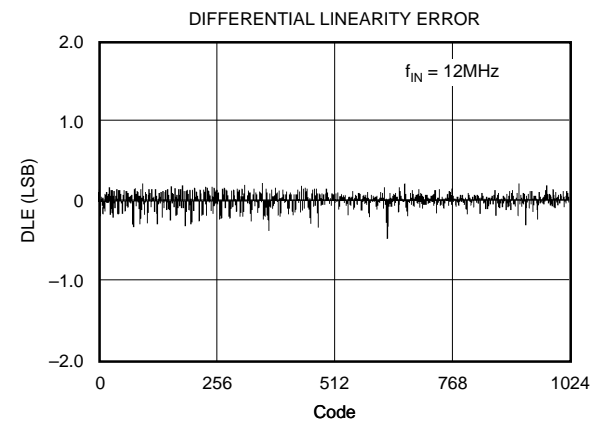
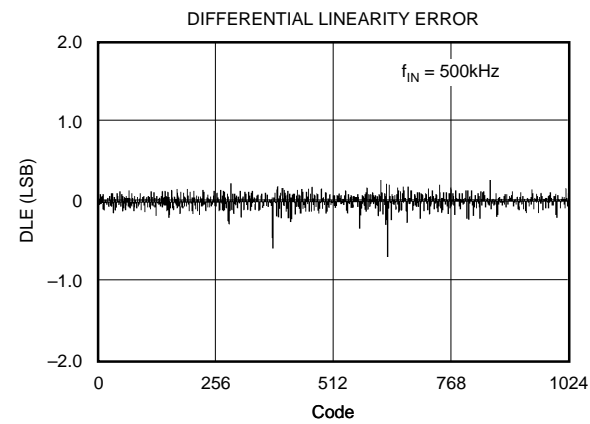
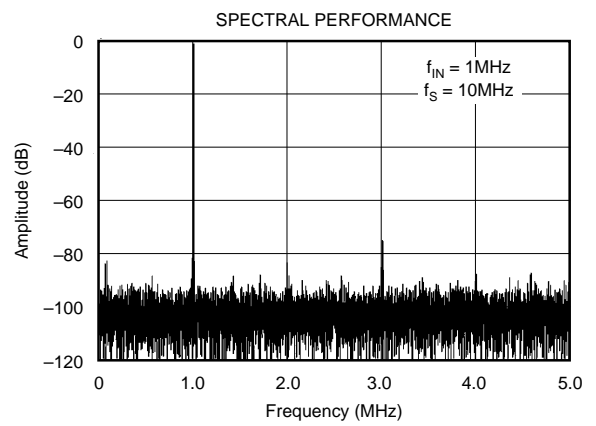
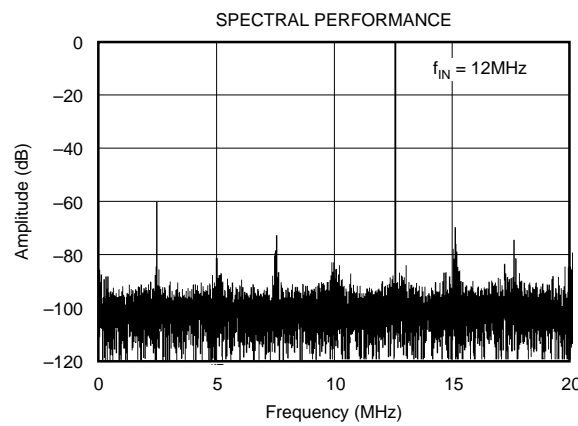
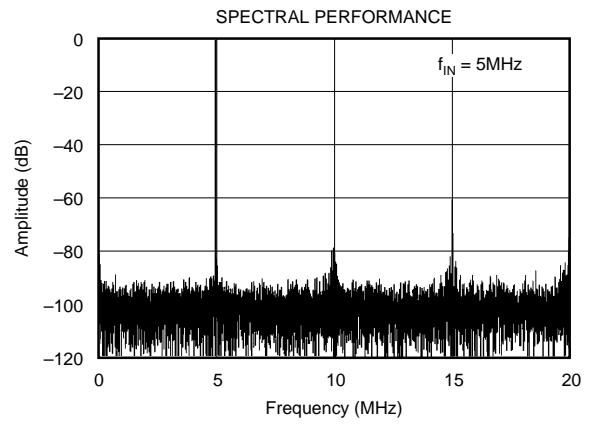
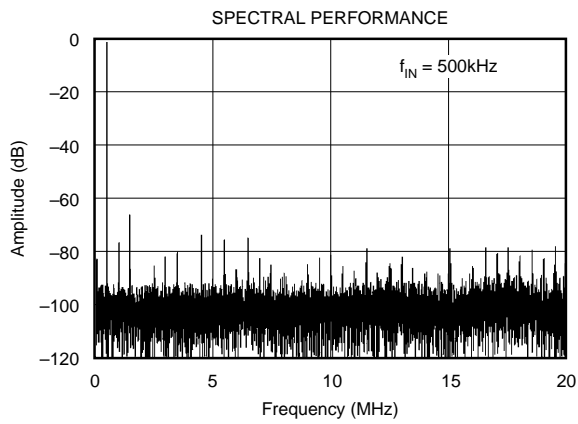
PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10, Least Significant Bit
12	DNC	Do not connect.
13	DNC	Do not connect.
14	GND	Ground
15	+V _S	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	+V _S	+5V Power Supply
18	OE	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor.
20	+V _S	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	+V _S	+5V Power Supply
25	GND	Ground
26	IN	Input
27	IN	Complementary Input
28	GND	Ground

TIMING DIAGRAM



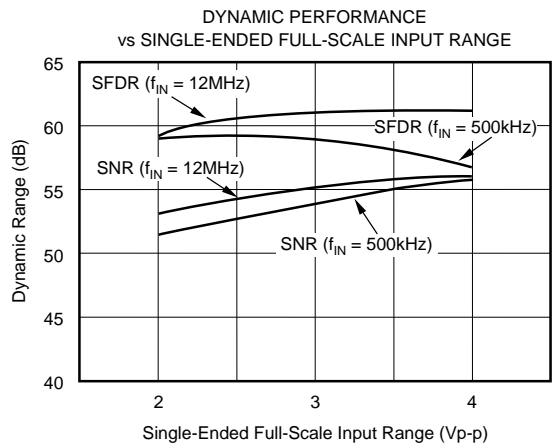
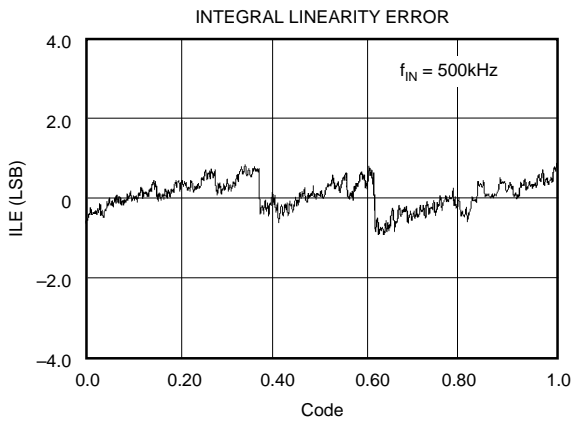
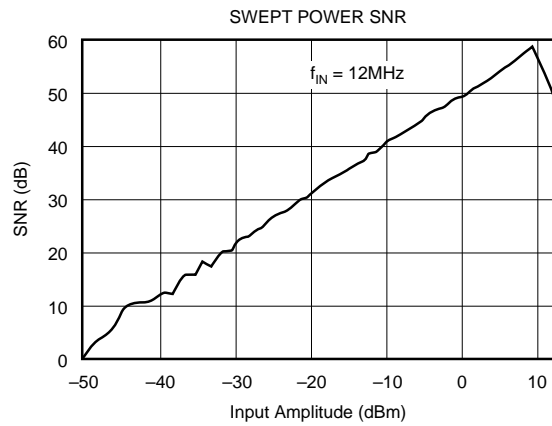
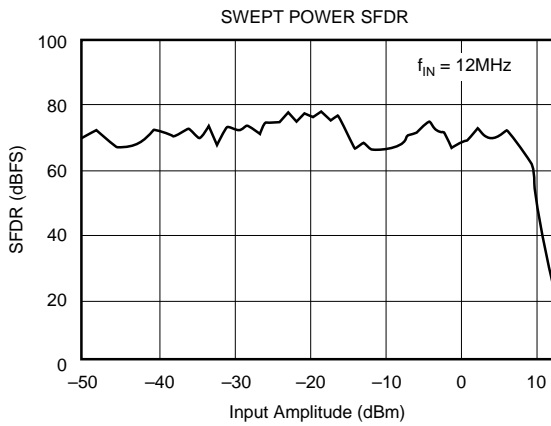
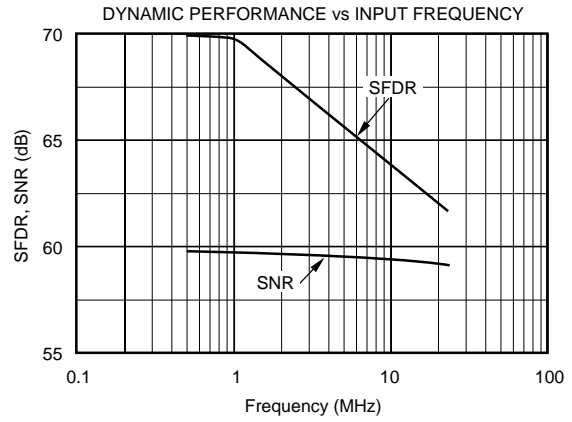
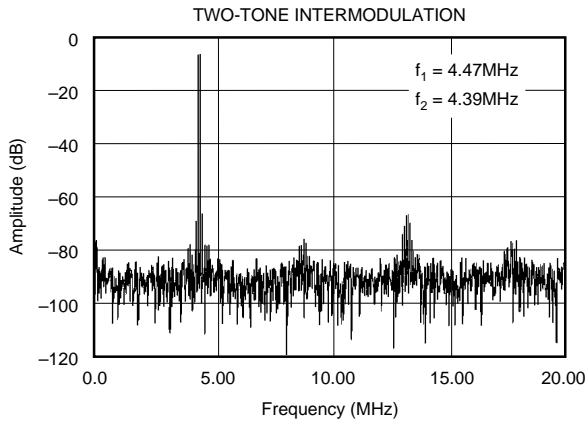
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

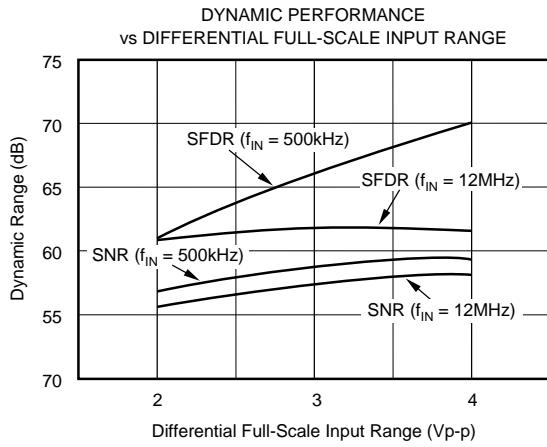
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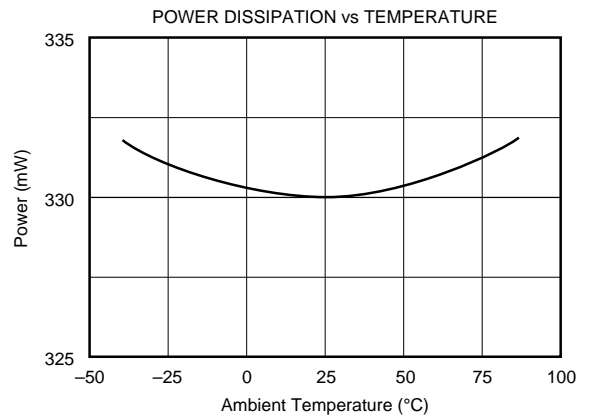
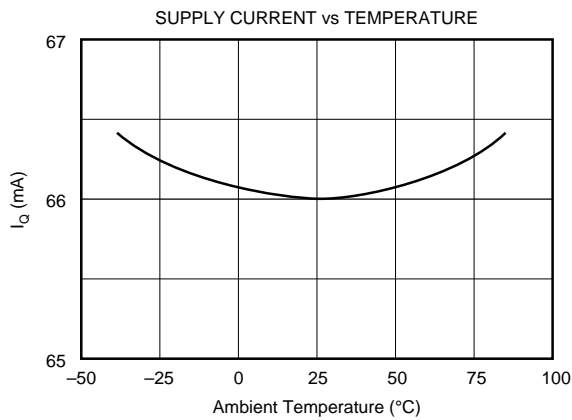
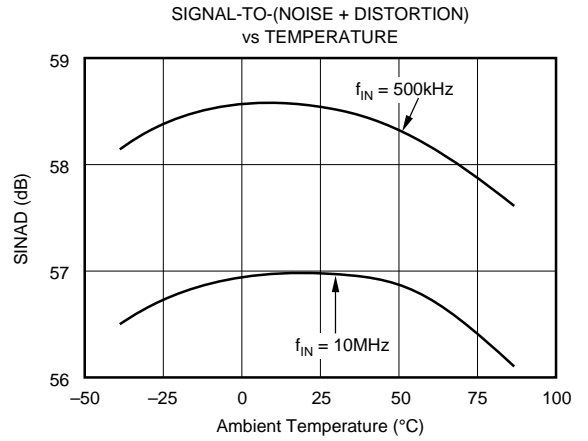
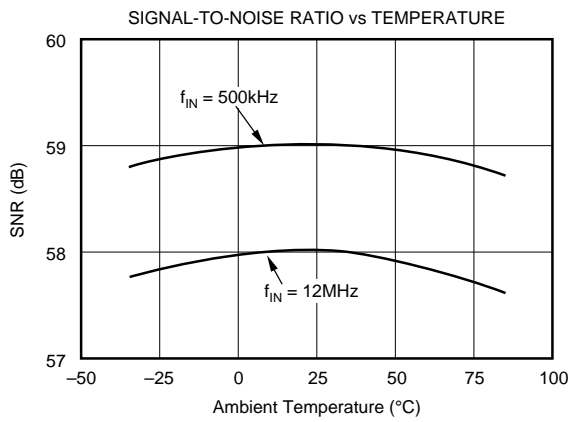
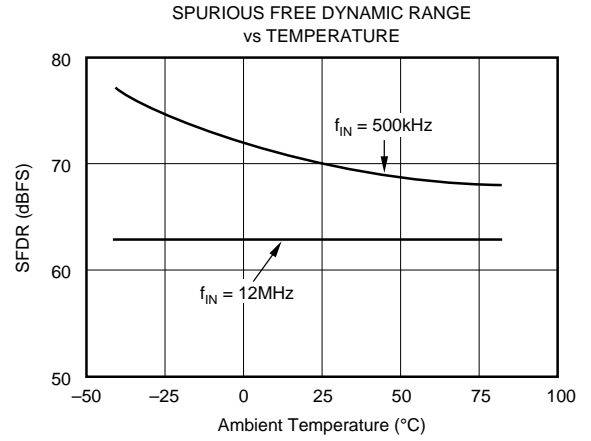
NOTE: REFT_{EXT} varied, REFB is fixed at the internal value of +1.25V.

TYPICAL PERFORMANCE CURVES (CONT)

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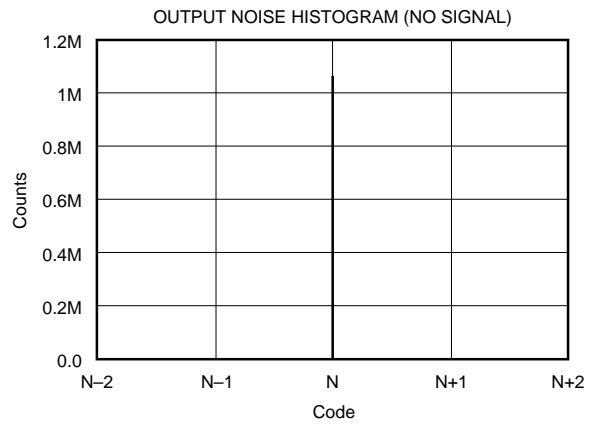
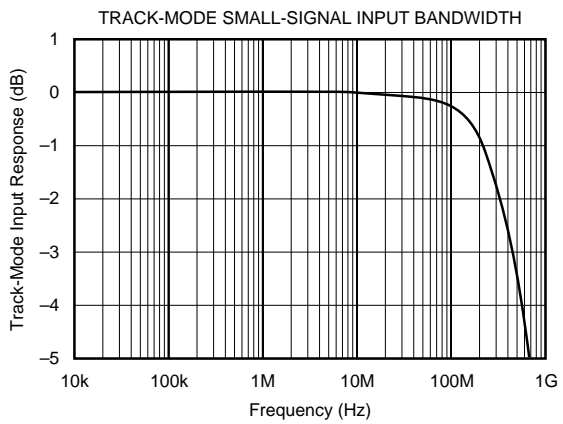
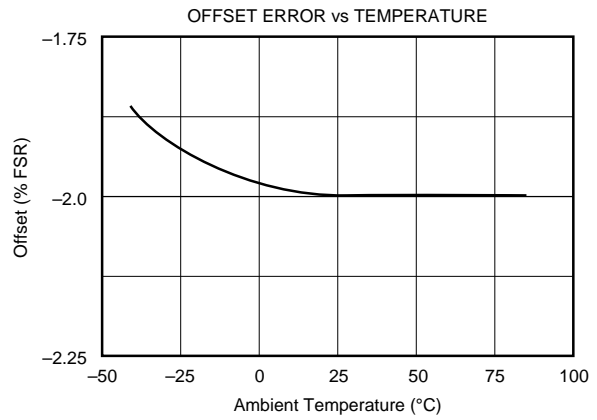
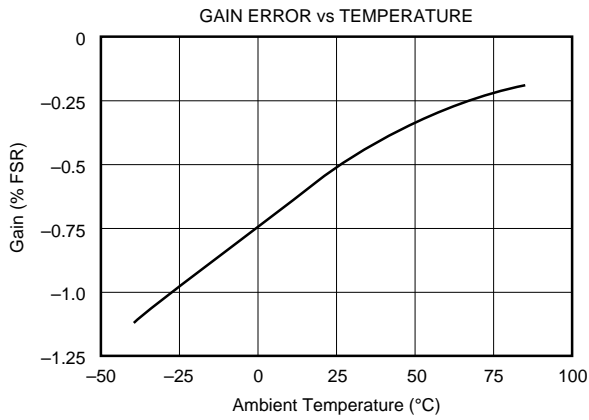


NOTE: REFT_{EXT} varied, REFB is fixed at internal value of +1.25V.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.



THEORY OF OPERATION

The ADS821 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 10-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_1 and C_H , completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

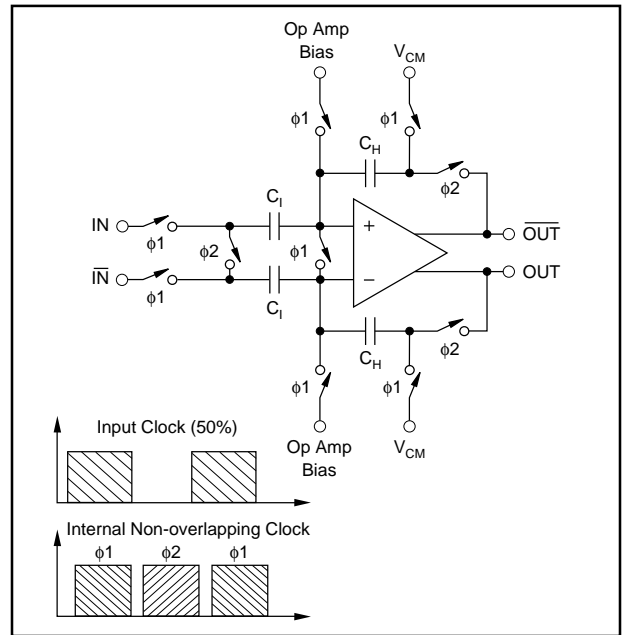


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

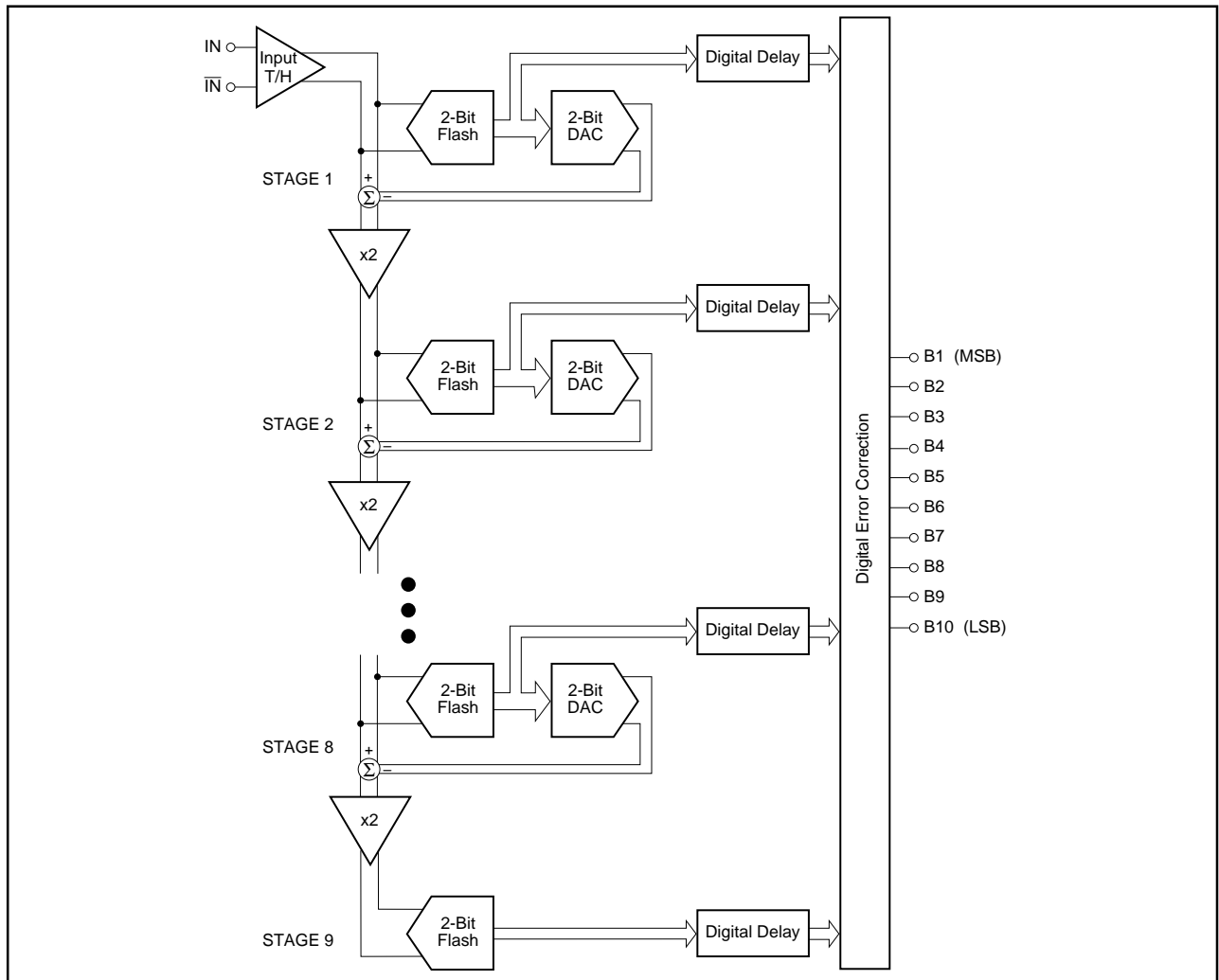


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS821 excellent differential linearity and guarantees no missing codes at the 10-bit level.

The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS821 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS821 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale reference (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended inputs, and ADS821 drive circuits, refer to the applications section.

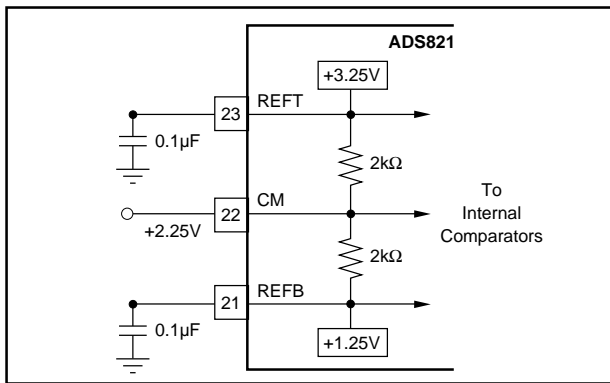


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock control the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise/fall times and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise and fall times** should be as short as possible (<2ns for best performance).

- For most applications, the clock duty should be set to 50%. However, for applications requiring no missing codes, a slight skew in the duty cycle will improve DNL performance for conversion rates >35MHz and input frequencies <2MHz (see Timing Diagram) in the SOIC package. For the best performance in the SSOP package, the clock should be skewed under all input frequencies with conversion rates >35MHz. A possible method for skewing the 50% duty cycle source is shown in Figure 4.

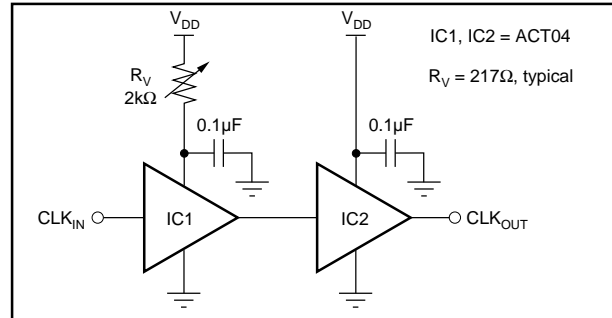


FIGURE 4. Clock Skew Circuit.

DIGITAL OUTPUT DATA

The 10-bit output data is provided at CMOS logic levels. There is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a high voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS821 can be set to a high impedance state by driving \overline{OE} (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

DIFFERENTIAL INPUT ⁽¹⁾	OUTPUT CODE	
	SOB PIN 19 FLOATING or LO	BTC PIN 19 HI
+FS (IN = +3.25V, \overline{IN} = +1.25V)	1111111111	0111111111
+FS -1LSB	1111111111	0111111111
+FS -2LSB	1111111110	0111111110
+3/4 Full Scale	1110000000	0110000000
+1/2 Full Scale	1100000000	0100000000
+1/4 Full Scale	1010000000	0010000000
+1LSB	1000000001	0000000001
Bipolar Zero (IN = \overline{IN} = +2.25V)	1000000000	0000000000
-1LSB	0111111111	1111111111
-1/4 Full Scale	0110000000	1110000000
-1/2 Full Scale	0100000000	1100000000
-3/4 Full Scale	0010000000	1010000000
-FS +1LSB	0000000001	1000000001
-FS (IN = +1.25V, \overline{IN} = +3.25V)	0000000000	1000000000

Note: In the single-ended input mode, +FS = +4.25V and -FS = +0.25V.

TABLE I. Coding Table for the ADS821.

APPLICATIONS

DRIVING THE ADS821

The ADS821 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage (CM) of +2.25V per Figure 5. This transformer-coupled input arrangement provides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5μA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{\text{IN}}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

Figure 6 shows an AC-coupled single-ended input interface circuit using the low cost, current feedback OPA658 as the active gain stage. When testing this configuration in gains of +4, +5.8 and +8.2, it was noted that reducing the feedback

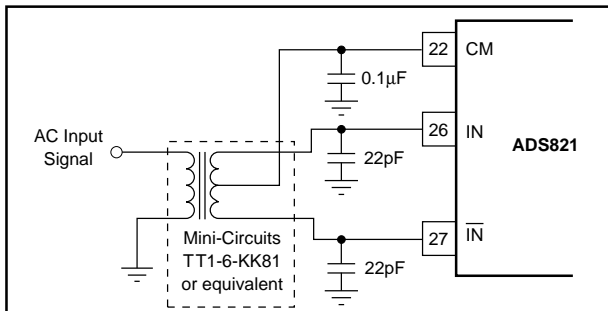


FIGURE 5. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

resistor of the OPA658 from the typical 402Ω to 360Ω resulted in a wider bandwidth, thus improving distortion at higher gains. The gain resistor was scaled to 120Ω, 75Ω and 50Ω for each of the three gain settings. The two 330Ω resistors set the RC time constant and the values can be varied, although higher values will have the effect of moving the corner frequency of the created high-pass filter down. In Figure 6, the -3dB point is set at 4.2kHz.

Figure 7 illustrates another possible low cost interface circuit which utilizes resistors and capacitors in place of a transformer. Depending on the signal bandwidth, the component values should be carefully selected in order to maintain the performance outlined in the data sheet. The input capacitors, C_{IN} , and the input resistors, R_{IN} , create a high-pass filter with the lower corner frequency at $f_c = 1/(2\pi R_{\text{IN}} C_{\text{IN}})$. The corner frequency can be reduced by either increasing the value of R_{IN} or C_{IN} . If the circuit operates with a 50Ω or 75Ω impedance level, the resistors are fixed and only the value of the capacitor can be increased. Usually AC-coupling capacitors are electrolytic or tantalum capacitors with values of 1μF or higher. It should be noted that these large capacitors become inductive with increased input frequency, which could lead to signal amplitude errors or oscillation. To maintain a low AC-coupling impedance throughout the signal band, a small value (e.g. 1μF) ceramic capacitor could be added in parallel with the polarized capacitor.

Capacitors C_{SH1} and C_{SH2} are used to minimize current glitches resulting from the switching in the input track and hold stage and to improve signal-to-noise performance. These capacitors can also be used to establish a low-pass filter and effectively reduce the noise bandwidth. In order to create a real pole, resistors R_{SER1} and R_{SER2} were added in series with each input. The cut-off frequency of the filter is determined by $f_c = 1/(2\pi R_{\text{SER}}(C_{\text{SH}} + C_{\text{ADC}}))$ where R_{SER} is the resistor in series with the input, C_{SH} is the external capacitor from the input to ground, and C_{ADC} is the internal input capacitance of the A/D converter (typically 4pF).

Resistors R_1 and R_2 are used to derive the necessary common mode voltage from the buffered top and bottom references.

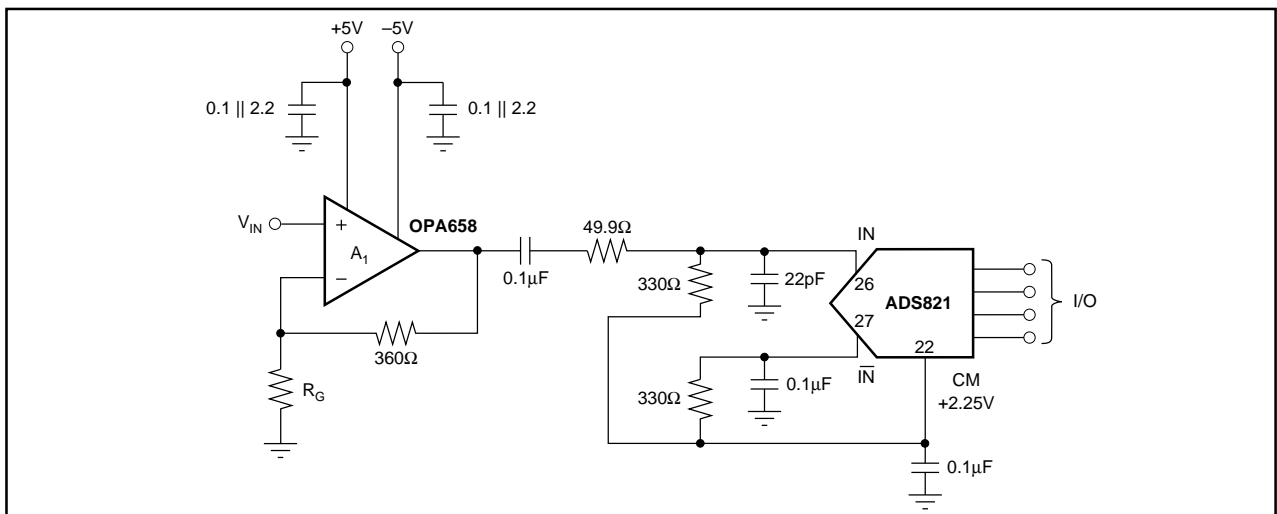


FIGURE 6. Low-Cost AC-Coupled Single-Ended Input Circuit.

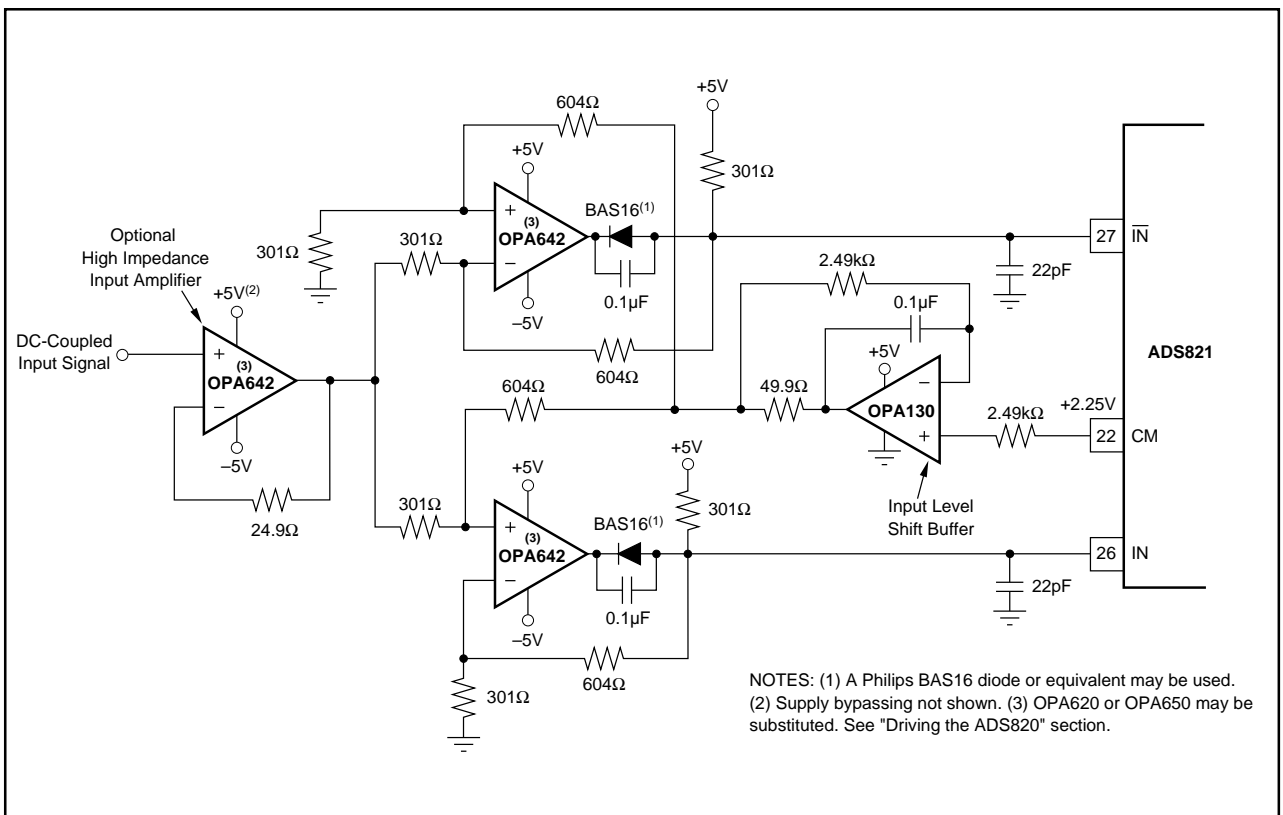


FIGURE 8. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

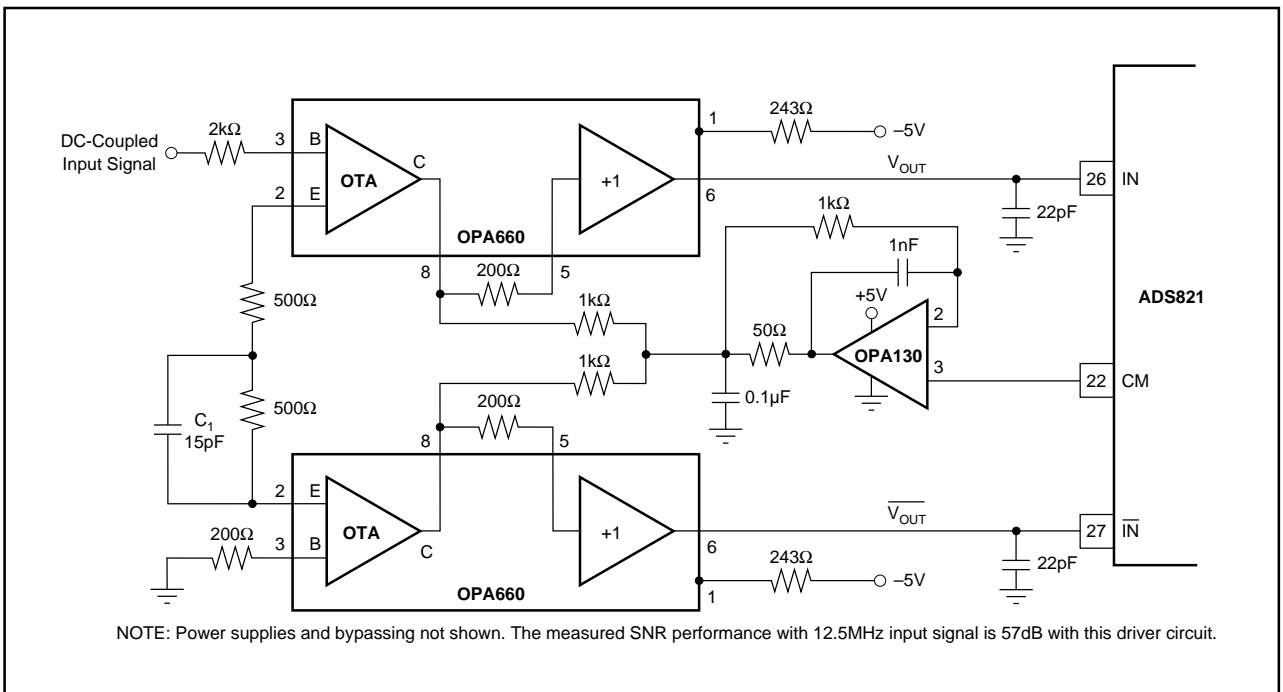


FIGURE 9. A Wideband DC-Coupled, Single-Ended to Differential Input Driver Circuit.

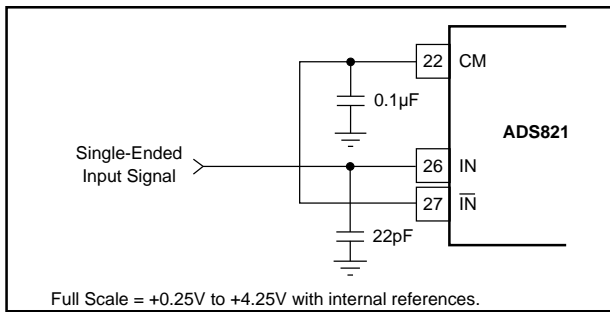


FIGURE 10. Single-Ended Input Connection.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS821 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS821 is a high performance converter and careful attention to test techniques is necessary to achieve accurate

results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS821. Using a signal amplitude slightly lower than full scale will allow a small amount of “headroom” so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2 . Five “bins” either side of peak are used for calculation of fundamental and harmonic power. The “0” frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

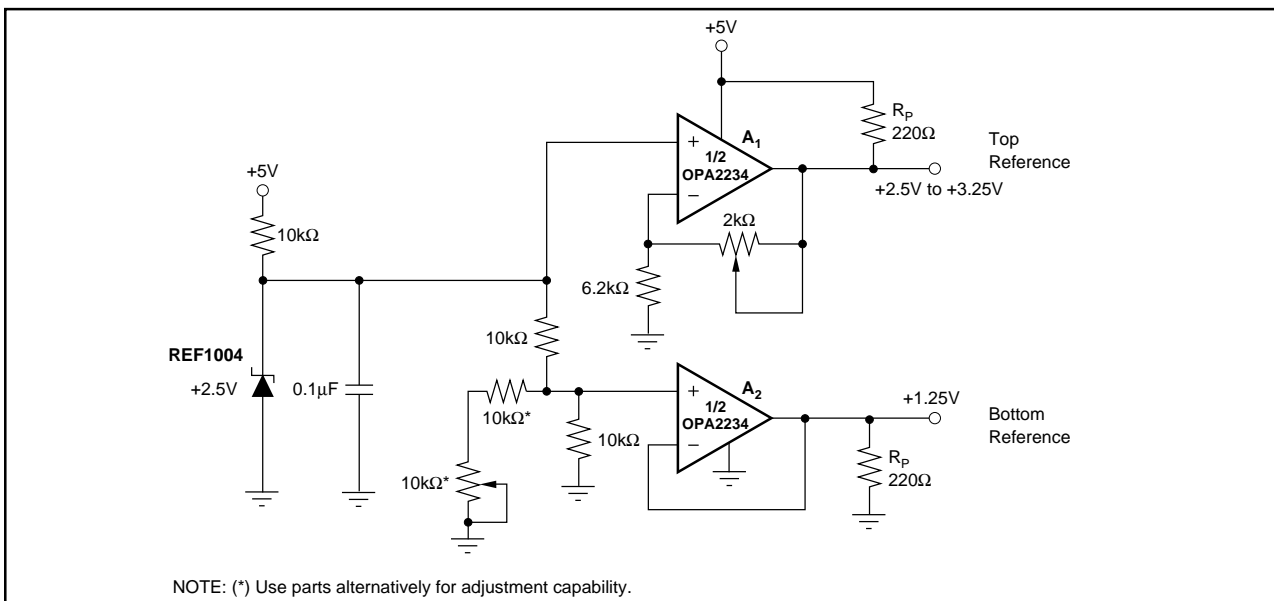


FIGURE 11. Optional External Reference to Set the Full-Scale Range Utilizing a Dual, Single-Supply Op Amp.

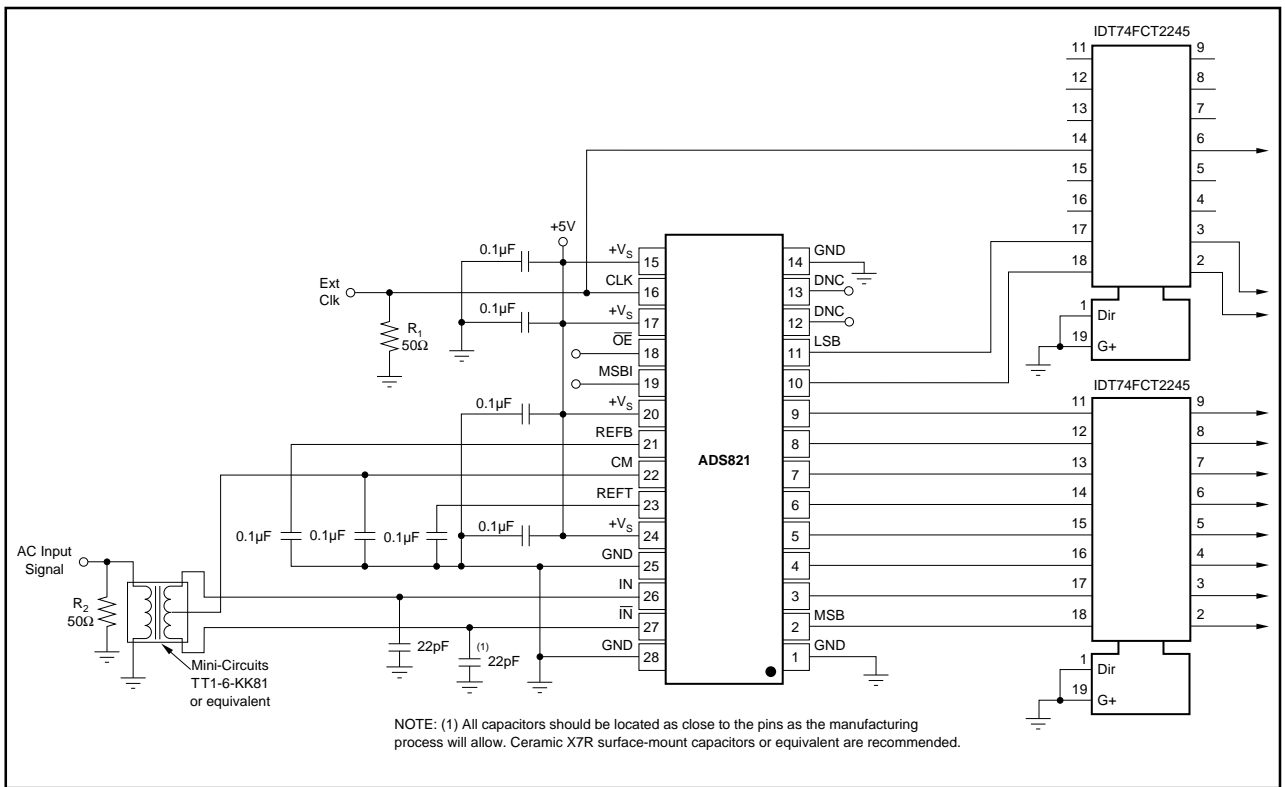


FIGURE 12. ADS821 Interface Schematic with AC-Coupling and External Buffers.