BURR - BROWN®

ADS7833

10-Channel, 12-Bit DATA ACQUISITION SYSTEM

FEATURES

- 3 SIMULTANEOUS SAMPLED CHANNELS
- 3 SYNCHRONIZED 12-BIT ADCs
- 6.6µs THROUGHPUT RATE
- FULLY DIFFERENTIAL MUX INPUTS
- DIGITALLY SELECTABLE INPUT RANGES
- ±5V POWER SUPPLIES
- SERIAL DIGITAL INPUT/OUTPUTS
- 2 SIMULTANEOUS SAMPLED AUXILIARY CHANNELS
- DIRECT INTERFACE TO MOTOROLA'S DSP56004/7

APPLICATIONS

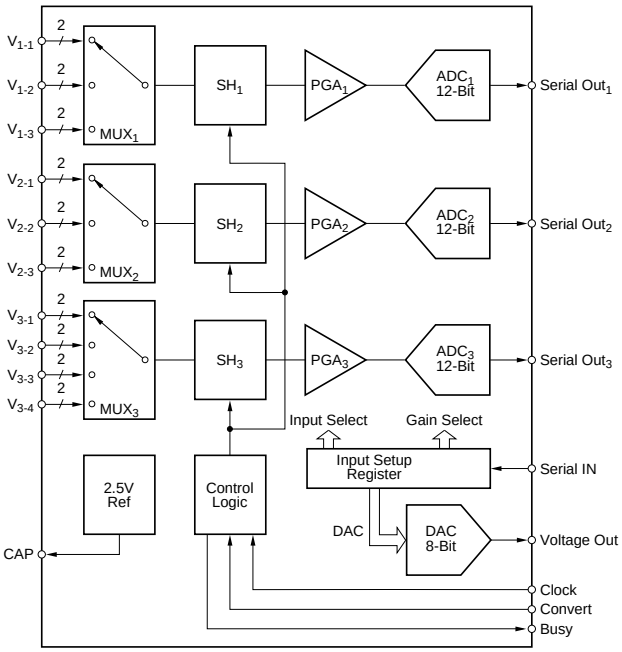
- AC MOTOR SPEED CONTROLS
- THREE PHASE POWER CONTROL
- UNINTERRUPTABLE POWER SUPPLIES
- VIBRATION ANALYSIS
- PC DATA ACQUISITION
- MEDICAL INSTRUMENTATION

DESCRIPTION

The ADS7833 consists of three 12-bit analog-to-digital converters preceded by three simultaneously operating sample-hold amplifiers, and multiplexers for 10 differential inputs. The ADCs have simultaneous serial outputs for high speed data transfer and data processing.

The ADS7833 also offers a programmable gain amplifier with programmable gains of 1.0V/V, 1.25V/V, 2.5V/V, and 5.0V/V. Channel selection and gain selection are selectable through the serial input control word. The high through put rate is maintained by simultaneously clocking in the 13-bit input control word for the next conversion while the present conversions are clocked out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1235C
Printed in U.S.A. May, 1997

SPECIFICATIONS

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 2.1MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
RESOLUTION		12			Bit
ANALOG INPUT					
Full Scale Voltage, Differential	G = 1.0V/V		±2.5		V
	G = 1.25V/V		±2.0		V
	G = 2.5V/V		±1.0		V
	G = 5.0V/V		±0.5		V
Common-Mode Voltage		±0.5	See Table VII		V
Impedance			10^{12}		Ω
Capacitance			20		pF
THROUGHPUT SPEED					
Conversion Time	CLK = 2.1MHz			6.1	µs
Complete Cycle	Acquire and Convert			6.6	µs
Throughput Rate		150	200		kHz
SAMPLING DYNAMICS					
S/H Droop Rate			0.1		µV/µs
S/H Acquisition Time			0.5		µs
S/H Aperture Delay			50		ns
S/H Aperture Jitter			50		ps
Sampling Skew, Channel-to-Channel			3		ns
DC ACCURACY					
Integral Linearity - ADC			±0.5	±2	LSB
Differential Linearity - ADC			±0.5		LSB
No Missing Codes		12			Bits
Integral Linearity - Asynchronous, Synchronous			0.5	±3	LSB
Differential Linearity - Asynchronous, Synchronous			0.5	±3	LSB
Full Scale Error	G = 1.0V/V			2	% of FSR
Full Scale Error Other Gains				4	% of FSR
Full Scale Error Drift	G = 1.0V/V		±10	±100	ppm/°C
	G = 2.5V/V		±10	±100	ppm/°C
Zero Error - ADC	G = 1.0V/V		±0.5	±15	LSB
Zero Error - Asynchronous, Synchronous	G = 1.0V/V		±0.5	±20	LSB
Zero Error Drift	G = 1.0V/V		±0.5		ppm/°C
AC ACCURACY					
Total Harmonic Distortion					
f_{IN} = 1kHz			92		dB
f_{IN} = 1MHz			72		dB
CMR	V_{CM} = 1V, f_{CM} = 1MHz		40		dB
REFERENCE					
Internal Reference Voltage			2.5		V
Internal Reference Accuracy			±0.25		%
Internal Reference Drift			±10		ppm/°C
Internal Reference Source Current			10		µA
External Reference Voltage Range for Specified Linearity		2.25	2.5	2.75	V
External Reference Current Drain			10		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		0		1.5	V
V_{IH}		+3.5		+5	V
I_{IL}				±10	µA
I_{IH}				±10	µA
Input Capacitance	At All Digital Input Pins			15	pF
DIGITAL OUTPUTS					
Data Format			12-Bit Serial		
Data Coding			BTC		
V_{OL}	I_{SINK} = 1.6mA	0		0.4	V
V_{OH}	I_{SOURCE} = 500µA	4.2		5	V
Leakage Current				±5	µA
Output Capacitance	At All Digital Output Pins			15	pF

SPECIFICATIONS (CONT)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 2.1MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
POWER SUPPLIES	Specified Performance				
V_{ANA+}		+4.75	+5.0	+5.25	V
V_{ANA-}		–4.75	–5.0	–5.25	V
V_{DIG+}		+4.75	+5.0	+5.25	V
V_{DIG-}		–4.75	–5.0	–5.25	V
I_{ANA+}			15	25	mA
I_{ANA-}			8	10	mA
I_{DIG+}			3	5	mA
I_{DIG-}			1	2	mA
Power Dissipation			125		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Derated Performance		–55		+125	°C
Storage		–65		+150	°C

DIGITAL-TO-ANALOG CONVERTER

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
RESOLUTION		8-Bits			
Output Range		0		+2.5	V
Output Settling Time	To 0.5LSB			1	µs
Linearity Error				±1	LSB
Differential Linearity				±1	LSB
Output Current		200			µA
Offset Error			±1	10	mV
Full Scale Error				2	%

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage ..... ±25V
Ground Voltage Difference: AGND and DGND ..... ±0.3V
Power Supply Voltages:
V_{ANA+} ..... +7V
V_{ANA-} ..... –7V
V_{DIG+} ..... +7V
V_{DIG-} ..... –7V
Digital Inputs ..... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

CONVERSION AND DATA TIMING

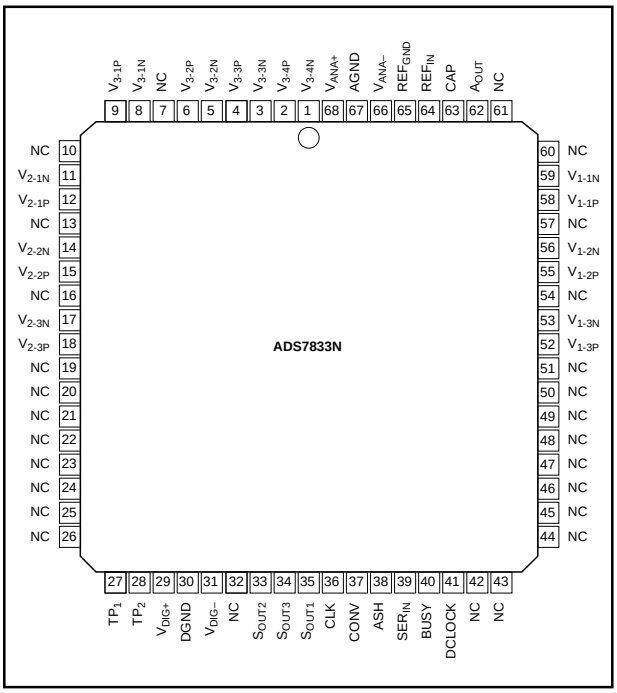
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	A/D Conversion Time	6.6	4.0		µs
CLK	A/D Conversion Clock	2.1	2.8		MHz
t_1	Setup Time for Conversion Before Rising Edge of Clock	50			ns
t_2	Hold Time for Conversion After Rising Edge of Clock	50			ns
t_3	Setup Time for Serial Out			25	ns
t_4	Setup Time for Serial Input	30			ns
t_5	Hold Time for Serial Input	30			ns

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7833N	68-Lead PLCC	312

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



PIN DEFINITIONS

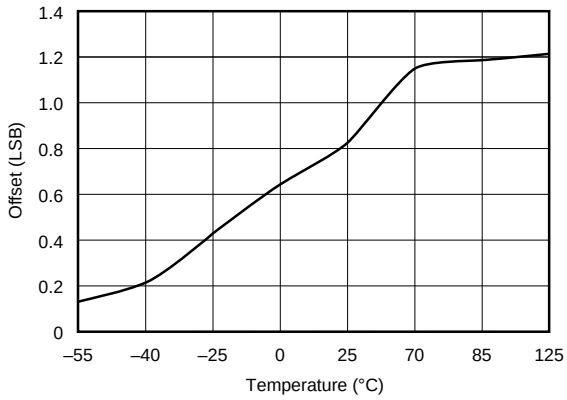
PIN NO	NAME	TYPE[1]	DESCRIPTION	PIN NO	NAME	TYPE[1]	DESCRIPTION
1	V_{3-4N}	AI	Voltage Input, Channel 3, Mux I/P 4, Negative Side	35	S_{OUT1}	DO	Serial Digital Output, Channel 1
				36	CLK	DI	Clock for A/D Converters
2	V_{3-4P}	AI	Voltage Input, Channel 3, Mux IP 4, Positive Side	37	CONV	DI	Start A/D Converters. When CONV goes to "0" (low) the next rising edge of CLK starts the conversion.
3	V_{3-3N}	AI	Voltage Input, Channel 3, Mux I/P 3, Negative Side	38	ASH	DI	Digital Control for Asynchronous Sample Hold. If signal is "1" (high), signals are sampled.
4	V_{3-3P}	AI	Voltage Input, Channel 3, Mux I/P 3, Positive Side				
				39	SER_{IN}	DI	Serial Digital Input for Input Control Word
5	V_{3-2N}	AI	Voltage Input, Channel 3, Mux I/P 2, Negative Side	40	BUSY	DO	A/D Converters Busy. Busy if signal is "0" (low).
6	V_{3-2P}	AI	Voltage Input, Channel 3, Mux I/P 2, Positive Side	41	DCLOCK	DO	A Delayed and Truncated Version of the CLK Signals. It is Delayed 50ns from the CLK Signal and Stays Low after 13 DCLOCK Cycles.
7	NC	—	No Connection				
8	V_{3-1N}	AI	Voltage Input, Channel 3, Mux I/P 1, Negative Side				
				42	NC	—	No Connection
9	V_{3-1P}	AI	Voltage Input, Channel 3, Mux I/P 1, Positive Side	43	NC	—	No Connection
				44	NC	—	No Connection
10	NC	—	No Connection	45	NC	—	No Connection
11	V_{2-1N}	AI	Voltage Input, Channel 2, Mux I/P 1, Negative Side	46	NC	—	No Connection
				47	NC	—	No Connection
12	V_{2-1P}	AI	Voltage Input, Channel 2, Mux I/P 1, Positive Side	48	NC	—	No Connection
				49	NC	—	No Connection
13	NC	—	No Connection	50	NC	—	No Connection
				51	NC	—	No Connection
14	V_{2-2N}	AI	Voltage Input, Channel 2, Mux I/P 2, Negative Side	52	V_{1-3P}	AI	Voltage Input, Channel 1, Mux I/P 3, Positive Side
15	V_{2-2P}	AI	Voltage Input, Channel 2, Mux I/P 2, Positive Side	53	V_{1-3N}	AI	Voltage Input, Channel 1, Mux I/P 3, Negative Side
16	NC	—	No Connection				
17	V_{2-3N}	AI	Voltage Input, Channel 2, Mux I/P 3, Negative Side.	54	NC	—	No Connection
				55	V_{1-2P}	AI	Voltage Input, Channel 1, Mux I/P 2, Positive Side
18	V_{2-3P}	AI	Voltage Input, Channel 2, Mux I/P 3, Positive Side	56	V_{1-2N}	AI	Voltage Input, Channel 1, Mux I/P 2, Negative Side
19	NC	—	No Connection				
20	NC	—	No Connection	57	NC	—	No Connection
21	NC	—	No Connection	58	V_{1-1P}	AI	Voltage Input, Channel 1, Mux I/P 1, Positive Side
22	NC	—	No Connection				
23	NC	—	No Connection	59	V_{1-1N}	AI	Voltage Input, Channel 1, Mux I/P 1, Negative Side
24	NC	—	No Connection				
25	NC	—	No Connection	60	NC	—	No Connection
26	NC	—	No Connection	61	NC	—	No Connection
27	TP1	—	Test Point 1, Make No Connection	62	A_{OUT}	AO	Output of DAC
28	TP2	—	Test Point 2, Make No Connection	63	CAP	AO	Decoupling Point for Internal Reference
29	V_{DIG+}	P	Digital Supply Voltage, +5V	64	REF_{IN}	AI	Input Pin for External Reference
30	DGND	P	Digital Supply Voltage, Ground	65	REF_{GND}	P	Ground Pin for External Reference
31	V_{DIG-}	P	Digital Supply Voltage, –5V	66	V_{ANA-}	P	Analog Supply Voltage, –5V
32	NC	—	No Connection	67	AGND	P	Analog Supply Voltage, Ground
33	S_{OUT2}	DO	Serial Digital Output, Channel 2	68	V_{ANA+}	P	Analog Supply Voltage, +5V
34	S_{OUT3}	DO	Serial Digital Output, Channel 3				

NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.

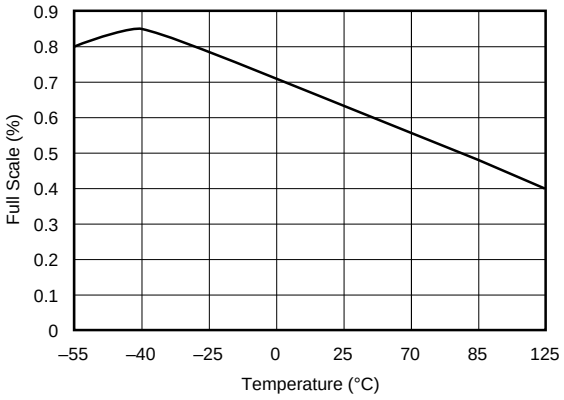
TYPICAL PERFORMANCE CURVES

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 2.1MHz.

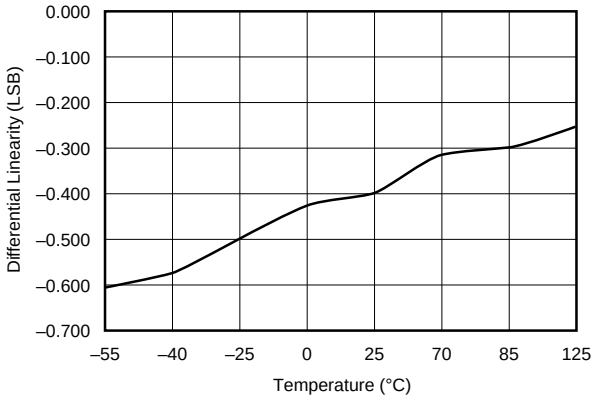
OFFSET vs TEMPERATURE



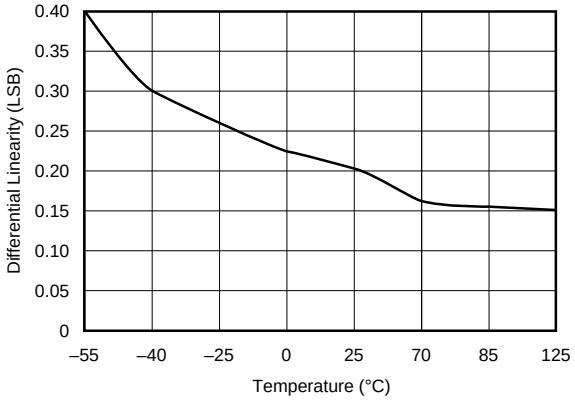
FULL SCALE vs TEMPERATURE



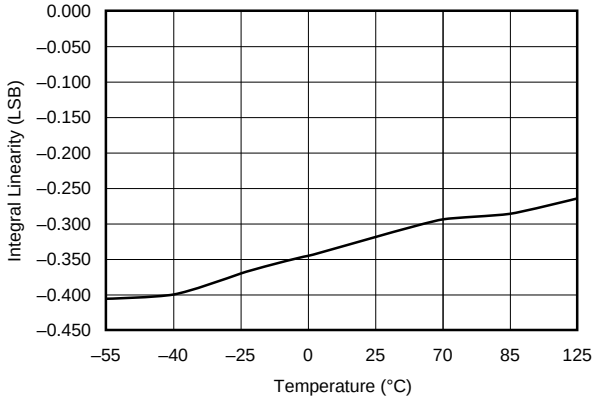
DIFFERENTIAL LINEARITY (MIN) vs TEMPERATURE



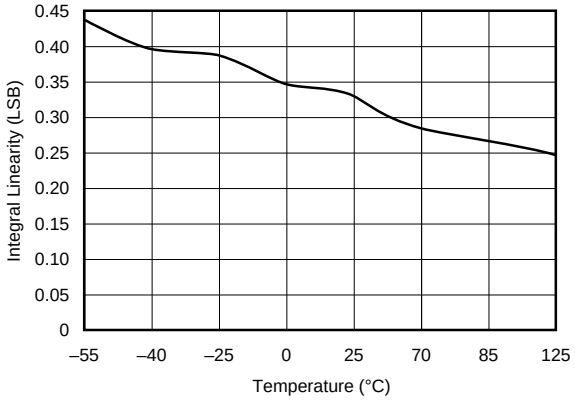
DIFFERENTIAL LINEARITY (MAX) vs TEMPERATURE



INTEGRAL LINEARITY (MIN) vs TEMPERATURE



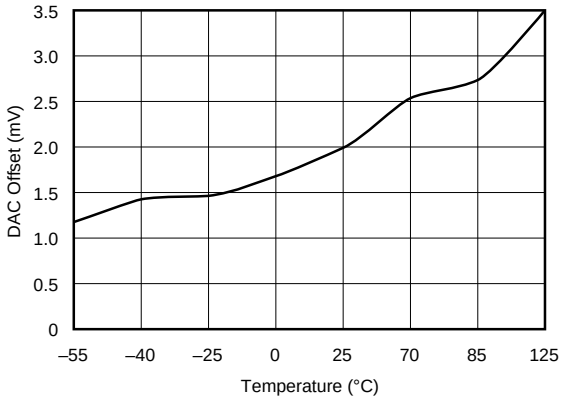
INTEGRAL LINEARITY (MAX) vs TEMPERATURE



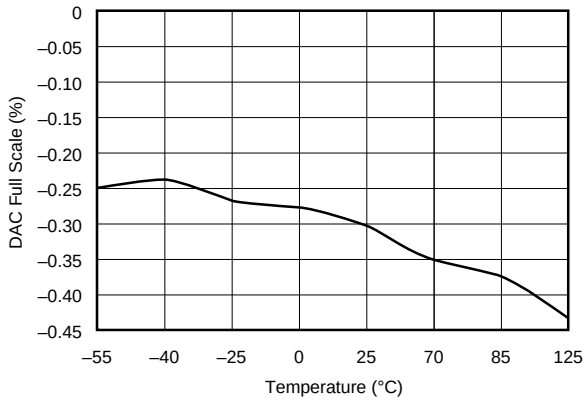
TYPICAL PERFORMANCE CURVES (CONT)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 2.1MHz.

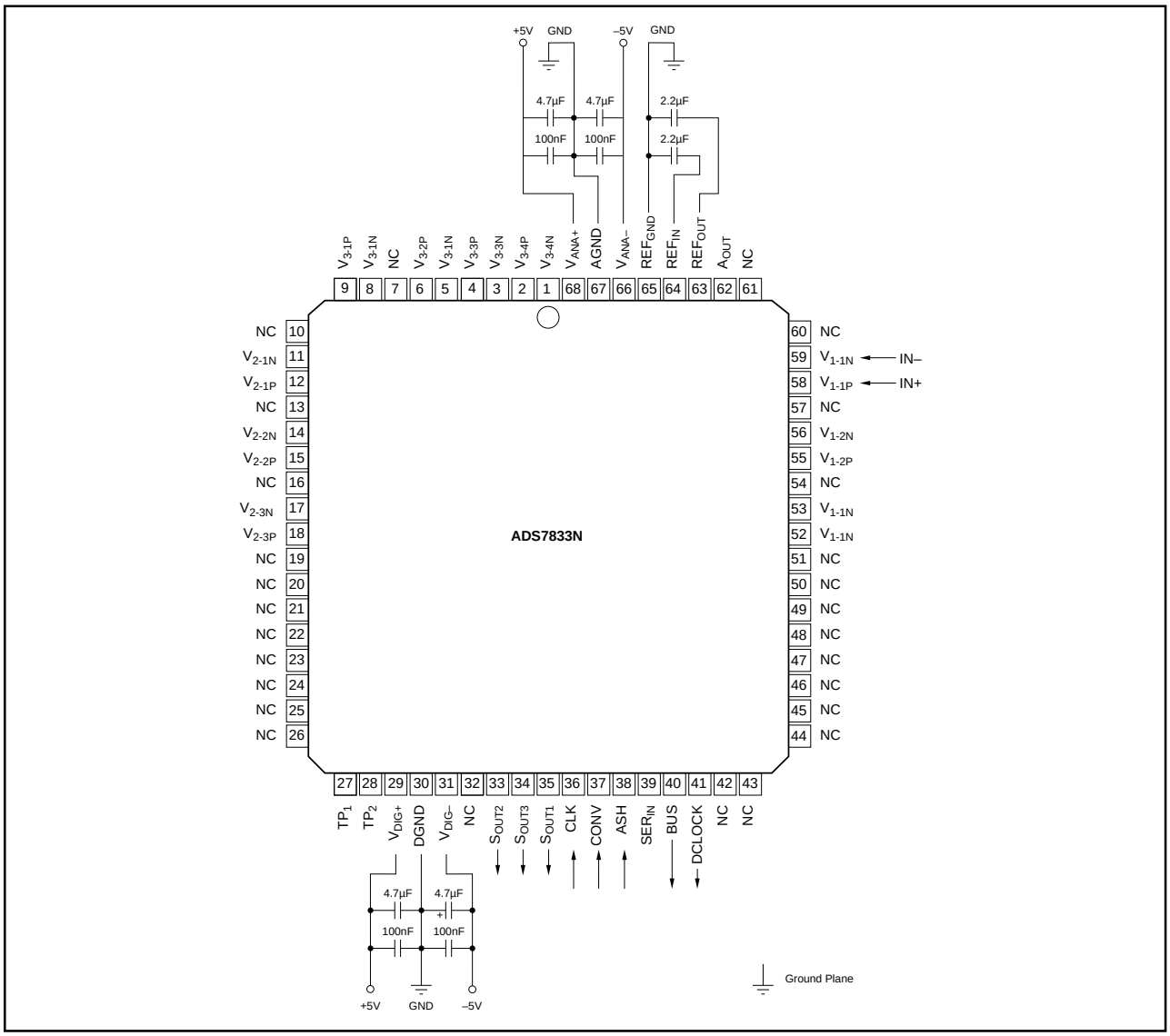
DAC OFFSET vs TEMPERATURE



DAC FULL SCALE vs TEMPERATURE



BASIC CIRCUIT CONFIGURATION



FUNCTIONAL DESCRIPTION

(See Figure 1)

ADCs AND PGAs

The ADS7833 contains three signal channels each with a 12-bit analog-to-digital converter output. The ADCs operate synchronously and their serial outputs occur simultaneously. (Table VI gives the analog input/digital output relationships). The ADCs are preceded by programmable gain amplifiers. (Table II gives gain select information). For channels one and two, the PGAs are effective for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3}, and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

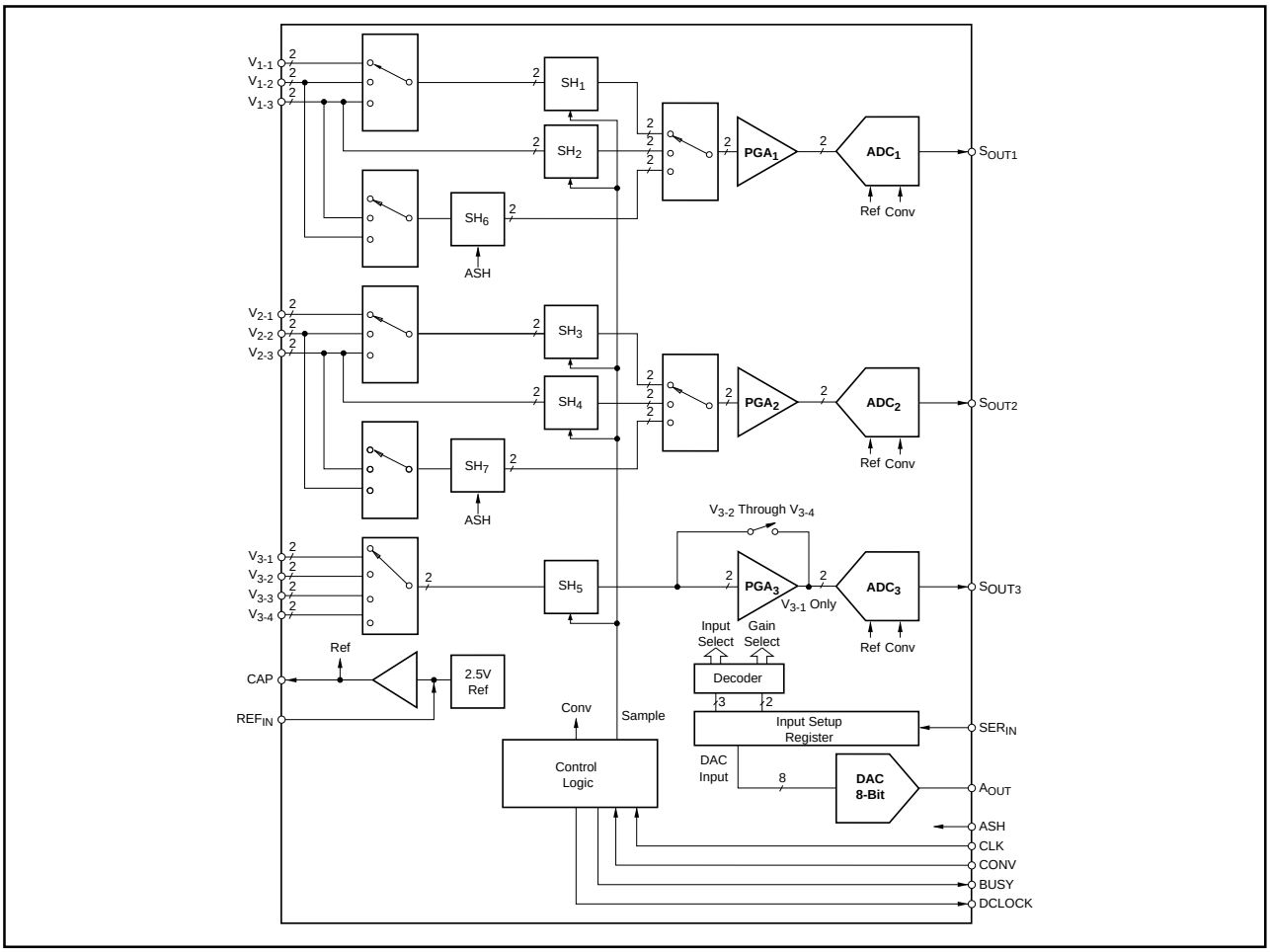


FIGURE 1. Functional Diagram.

SAMPLE HOLDS

The ADS7833 contains seven sample holds. Five of them (SH_1 through SH_5) sample simultaneously and have their sample/hold timing internally synchronized. (The timing is shown in Figure 2).

Three of the sample holds (SH_1, SH_3, and SH_5) are connected to the input multiplexers so that they can provide simultaneous sampling for all of their channels inputs. In addition, SH_2 and SH_4 simultaneously sample the third input of their channels (V_{1-3} and V_{2-3}, respectively). This is useful in motor control applications where V_{1-2} and V_{1-3} are the quadrature inputs for one position sensor, and V_{2-2} and V_{2-3} are the quadrature inputs for a second position sensor (see Figure 6). In that application, it is desirable to sample the quadrature inputs of a given position sensor at the same time (even though they are converted on successive conversion cycles) (see Table III), so that their values are captured at the same shaft position.

The ADS7833 also has the capability for limited asynchronous sampling. The sampling of SH_6 and SH_7 is controlled asynchronously by the control signal ASH (see Table III). This allows two inputs each on channel 1 and channel 2 (see Table IV) to be sampled asynchronously from the timing of the other sample holds. This can be useful in motor control applications where the two inputs for each channel come from a position sensor and it is desired to sample based on position sensor timing rather than system clock timing.

MULTIPLEXERS

The ADS7833 also contains several multiplexers that are used to select the desired analog inputs and connect the proper sample hold outputs to the PGAs and ADCs. The MUXs are driven by a decoder which receives its inputs from the Input Setup Register. (See Table III and Table IV for information on input channel selection). The input multiplexers can take full differential input signals (see Figure 3 and Table VII). The analog signals stay differential through the sample holds and the PGAs all the way to the inputs of the ADSs. This is done to provide the best possible high frequency noise rejection.

INPUT SETUP

As the ADCs are converting and transmitted their serial digital data for one conversion cycle, a setup word is being received to be used for the next conversion cycle. The 13-bit word is supplied at the SER_{IN} pin (see Figure 1), and is stored in the buffered Input Setup Register. The Input Select and Gain Select portions of the word are decoded and determine the state of the multiplexers and PGAs (see CONFIGURABLE PARAMETERS section).

DIGITAL-TO-ANALOG CONVERTER

An 8-bit DAC provides 256 output voltage levels from 0V to 2.5V (see Table V for input/output relationships). The DAC is controlled by the DAC Input portion of the input setup word. The DAC Input portion of the word is strobed into the DAC at the end of the conversion cycle (14th CLK pulse in Figure 2).

VOLTAGE REFERENCE

The ADS7833 contains an internal 2.5V voltage reference. It is available externally through an output buffer amplifier. If it is desired to use an external reference, one may be connected at the REF_{IN} pins. This then overrides the internal 2.5V reference, is connected to the ADCs and is available buffered at the CAP pin.

OTHER DIGITAL INPUTS AND OUTPUTS

Sampling and conversion is controlled by the CONV input (see Figure 2). The ADS7833 is designed to operate from an external clock supplied at the CLK input. This allows the conversion to be done synchronously with system timing so that transient noise effects can be minimized. The CLK signal may run continuously or may be supplied only during convert sequences. The BUSY and DCLOCK signals are internally generated and are supplied to make interfaces with microprocessors easier (see Figures 2, 4, and 6).

CONFIGURABLE PARAMETERS

Configurable parameters are:

- PGA Gain
- Input multiplexer and sample/hold selection
- DAC output voltage

Configuration information for these parameters is contained in the SER_{IN} word (See Figure 2). As one conversion is taking place, the configuration for the next conversion is being loaded into the buffered Input Setup Register via the SER_{IN} word. Table I shows information regarding these parameters.

CLOCK POSITIONS(1)	DESCRIPTION	FUNCTIONS
2-9	DAC $Input_{0-7}$	Sets DAC Output Voltage
10-11	Gain $Select_{0-1}$	Sets PGA Gains
12-14	Input $Select_{0-2}$	Determines Multiplexers Conditions
NOTE: (1) See Figure 2. "Clock Pulse Reference No."		

TABLE I. Description of Configurable Parameters.

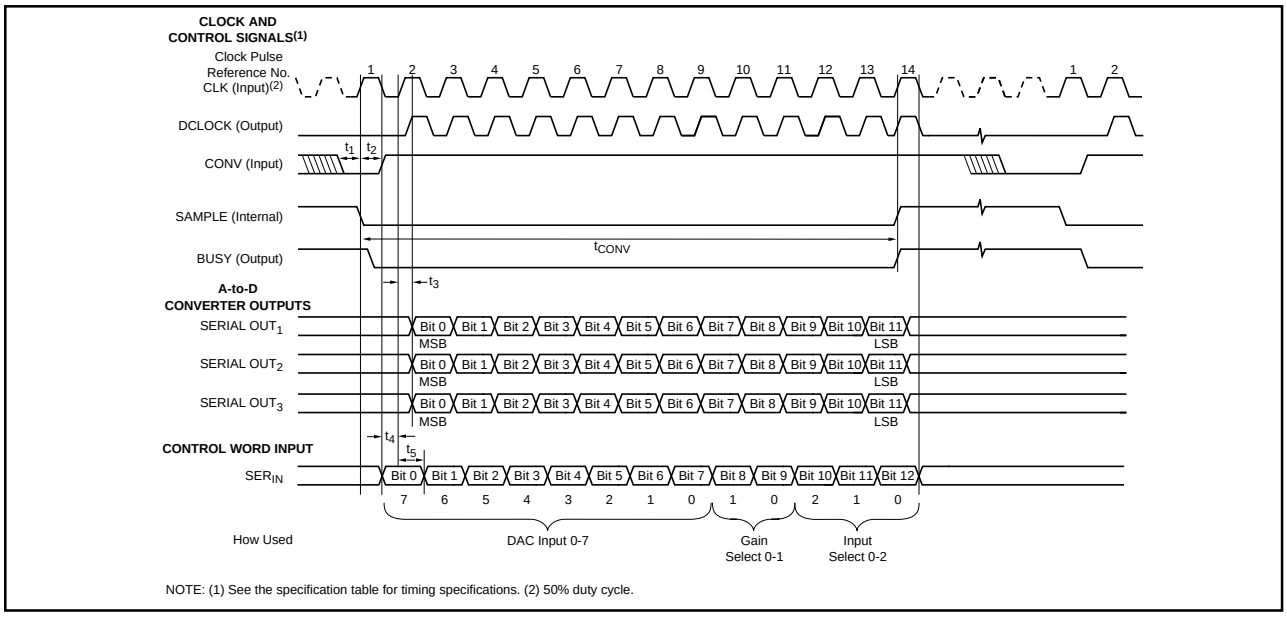


FIGURE 2. Timing Diagram.

PGA GAIN

The PGA gain is determined by the Gain Select portion (bits 8 and 9) in the SER_{IN} word (see Figure 2). There is one gain input that sets the same gain for all three PGAs. The gain values and allowable full scale inputs are shown in Table II.

For channels one and two the PGAs set the gain for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3} and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

GAIN $SELECT_{0-1}$	GAIN SETTING	FULL SCALE INPUT
0_H	5.0V/V	±0.5V
1_H	2.5V/V	±1.0V
2_H	1.25V/V	±2.0V
3_H	1.0V/V	±2.5V

TABLE II. Gain Select Information.

INPUT MULTIPLEXER AND SAMPLE HOLD SELECTION

The Input Select portion of the SER_{IN} word (bits 10, 11 and 12) (see Figure 2) are decoded and determine the open/closed condition of the multiplexer switches. This in turn determines which input signals are connected to the sample holds and which sample holds are connected to the PGAs/ADCs.

INPUT SIGNALS FOR PGAs/ADCs

Table III shows the relationships between the value of Input $Select_{0-2}$ and the signals that are converted.

INPUT $SELECT_{0-2}$		ANALOG SIGNAL CONNECTED TO PGA_X/ADC_X		
HEX CODE	BINARY CODE	PGA_1/ADC_1	PGA_2/ADC_2	PGA_3/ADC_2
0_H	000	Undefined	Undefined	V_{3-4}
1_H	001	V_{1-X} via SH_6(1)	V_{2-X} via SH_7(1)	V_{3-4}
2_H	010	V_{1-3} via SH_1	V_{2-3} via SH_3	V_{3-3}
3_H	011	V_{1-3} via SH_2	V_{2-3} via SH_4	V_{3-3}
4_H	100	V_{1-2}	V_{2-2}	V_{3-2}
5_H	101	V_{1-2}	V_{2-2}	V_{3-2}
6_H	110	V_{1-2}	V_{2-2}	V_{3-2}
7_H	111	V_{1-1}	V_{2-1}	V_{3-1}
NOTE: (1) See Table IV for Operation.				

TABLE III. Input Controls for Synchronous Sample Holds.

Input Select = 7_H—Synchronously sample and convert input signals V_{1-1}, V_{2-1}, and V_{3-1}.

Input Select = 4_H, 5_H, 6_H—Synchronously sample and convert input signals V_{1-2}, V_{2-2}, and V_{3-2}. These codes also cause SH_2 and SH_4 to sample their inputs. Values 4_H, 5_H, 6_H have different effects on the inputs to SH_6 and SH_7 (see Table IV).

Input Select = 3_H—Convert V_{1-3} via SH_2, V_{2-3} via SH_4, and V_{3-3} (V_{1-3} and V_{2-3} are from the value sampled in a preceding conversion cycle with Input Select = 4_H, 5_H or 6_H).

Input Select = 2_H—Convert V_{1-3} via SH_1, V_{2-3} via SH_3, and V_{3-3} (V_{1-3} is sampled on SH_2 in this conversion cycle).

Input Select = 1_H—Input V_{3-4} is converted by PGA_3/ADC_3. The output of the asynchronous sample holds, SH_6 and SH_7, are converted by PGA_1/ADC_1 and PGA_2/ADC_2, respectively. Note that the inputs to SH_6 and SH_7 are determined by previous Input Select values (see Table IV). Thus, to properly convert the output of one of the asynchronous sample holds it is first necessary to choose its input with a previous conversion cycle. Also, the output of SH_6 or SH_7 will only be converted if ASH goes low before the CONV command is received.

Input Select = 0_H—V_{3-4} is converted by PGA_3/ADC_3. The inputs to PGA_1/ADC_1 and PGA_2/ADC_2 are undefined.

CONVERSIONS FROM THE ASYNCHRONOUS SAMPLE HOLDS

Decoding the Input Select value also determines which inputs are applied to the two asynchronously controlled sample holds SH_6 and SH_7. (See Table IV.) One of the three possible inputs is selected by the Input Select value being 4, 5, or 6.

The "No Effect" states indicate that these values of Input Select have no effect on the multiplexers at the input of SH_6 and SH_7. When one of the "No Effect" values of Input Select is presented, the multiplexers will not be changed (i.e., their condition is determined by the last 4, 5, or 6 value of Input Select that existed prior to the "No Effect" state).

Note that Input Select = 1_H presents the output of SH_6 and SH_7 ($1ASH_X$ and $2ASH_X$) to PGA_1/ADC_1 and PGA_2/ADC_2, respectively (see Table III). Therefore, in order to properly convert the asynchronous sampled signals, it is first necessary to choose an input signal (Input Select equal 5 or 6 in Table IV) with one load/convert cycle and then convert the sample hold output (Input Select = 4 in Table III) in a following conversion cycle.

INPUT $SELECT_{0-2}$		ANALOG SIGNAL CONNECTED TO	
HEX CODE	BINARY CODE	SH_6	SH_7
0_H	000	No Effect	No Effect
1_H	001	No Effect	No Effect
2_H	010	No Effect	No Effect
3_H	011	No Effect	No Effect
4_H	100	Open	Open
5_H	101	V_{1-3}	V_{2-3}
6_H	110	V_{1-2}	V_{1-2}
7_H	111	No Effect	No Effect

TABLE IV. Input Controls for Asynchronous Sample Holds.

DAC OUTPUT VOLTAGE

The value of the DAC output voltage is determined by the DAC Input portion of the SER_{IN} word (bits 0 through 7—see Figure 2). The 8-bit DAC has 256 possible output voltages from 0V to +2.49V. The value of 1 LSB is 0.0098V.

ANALOG-TO-DIGITAL CONVERTERS

ARCHITECTURE

The ADCs are 12-bit, successive approximation types implemented with a switched capacitor circuitry.

SPEED

The clock for the ADC conversion is supplied externally at the CLK pin. Maximum clock frequency for specified accuracy is 2.1MHz. This results in a complete conversion cycle (S/H acquisition and A/D conversion) of 6.6µs.

INPUT/OUTPUT

The ADS7833 is designed for bipolar input voltages and uses a binary two's complement digital output code. A programmable gain function is associated with each ADC. This changes the full scale analog input range and the analog resolution of the converter. Details are shown in Table VI.

DIFFERENTIAL AND COMMON-MODE INPUT VOLTAGES

The ADS7833 is designed with full differential signal paths all the way from the multiplexer inputs through to the input of the ADCs. This was done to provide superior high frequency noise rejection.

DIGITAL INPUT DAC $INPUT_{0-7}$		ANALOG OUTPUT
HEX CODE	BINARY CODE	
00_H	0000 0000	0V
01_H	0000 0001	+0.0098V
•	•	•
•	•	•
•	•	•
FF_H	1111 1111	+2.499

TABLE V. DAC Input/Output Relationships.

As is common with most differential input semiconductor devices, there are compound restrictions on the combination of differential and common-mode input voltages. This matter is made slightly more complicated by the fact that most of the analog inputs are capable of being affected by the programmable gain function. The possible differential and single ended configurations are shown in Figures 3a and 3b.

The maximum differential and common mode restrictions are shown in Table VII.

GAIN SELECT CODE	0	1	2	3
Gain	5.0V/V	2.5V/V	1.25V/V	1.0V/V
Full Scale Range (V_D with V_{CM} = 0)	±0.5V	±1.0V	±2.0V	±2.5V
Largest Positive Common Mode Voltage, V_{CM}+	+2.7V	+2.4V	+1.9V	+1.6V
Largest Negative Common Mode Voltage, V_{CM}–	–2.7V	–2.4V	–1.9V	–1.6V

TABLE VII. Differential and Common Mode Voltage Restrictions.

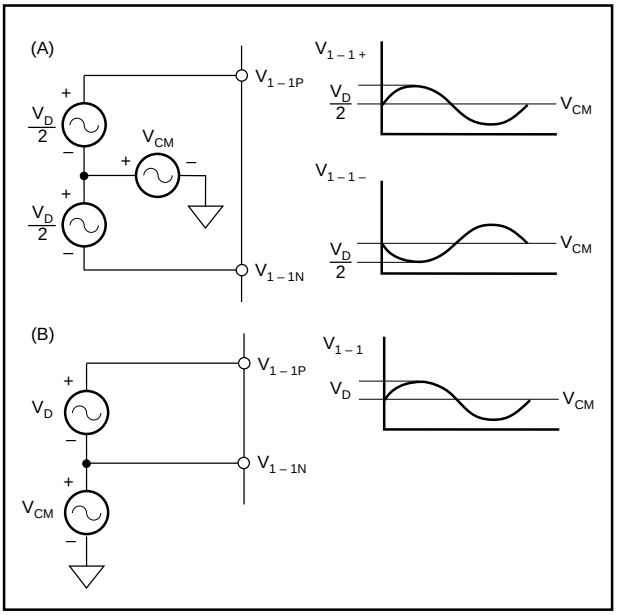


FIGURE 3. (a) Differential Signal Source, and (b) Single Ended Signal Source.

DESCRIPTION	ANALOG INPUT				DIGITAL OUTPUT	
GAIN SELECT CODE	0	1	2	3		
GAIN	5V/V	2.5V/V	1.25V/V	1.0V/V	BINARY TWO'S COMPLIMENT FORMAT	
FULL SCALE RANGE	±0.5V	±1.0V	±2.0V	±2.5V	HEX CODE	BINARY CODE
+Full Scale (FS –1LSB)	+0.49976	+0.9995V	+1.999V	+2.499	$7FF_H$	0111 1111 1111
One Bit above Mid-Scale	+0.244mV	+0.488mV	+0.976mV	+1.22mV	001H	0000 0000 0001
Mid-Scale	0V	0V	0V	0V	000_H	0000 0000 0000
One Bit Below Mid-Scale	–0.244V	–0.488mV	–0.976mV	–1.22mV	FFF_H	1111 1111 1111
–Full Scale	–0.500V	–1.000V	–2.000V	–2.500V	800_H	1000 0000 0000

NOTE: The programmable gain function applies to all three input channels for ADC_1 and ADC_2. However, the programmable gain function only applies to the first input (V_{3-1}) for ADC_3. The other three inputs (V_{3-2}, V_{3-3}, and V_{3-4}) are not affected by the GAIN SEL input. They operate at a fixed gain of 1V/V and thus have a fixed ±2.5V full scale input range.

TABLE VI. Analog Input - Digital Output Relationships.

MICROPROCESSOR INTERFACE

The internal logic of the ADS7833 is designed for easy control and data interface with microprocessors. Figure 4 shows the interface for loading the input control word from the microprocessor data bus into the serial input of the ADS7833.

Table VIII provides a sample assembly code and Figure 4 shows the connection diagram for connecting an ADS7833 to the DSP56004N—or DSP56007 a Motorola Digital Signal Processor. This configuration allows for full control of the ADS7833 as well as receiving all three conversion results simultaneously. The start of conversion is generated by the DSP56004 as well as the sample time of the asynchronous sample/holds.

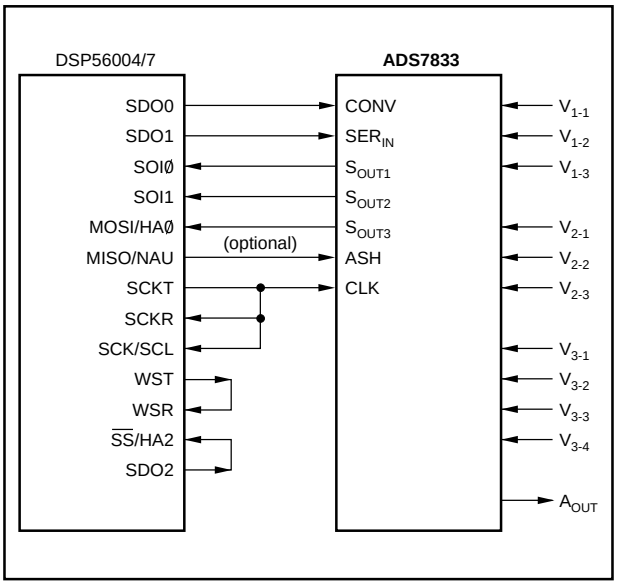


FIGURE 4. Microprocessor Interface for Motorola DSP56004/7.

While this is one of the most useful, the DSP56004/7 is flexible enough to allow various other configurations. These will free up the serial outputs for use with other serial peripherals, such as DACs.

TYPICAL ISOLATED ANALOG INPUT

Figure 5 shows an ISO130 used to isolate the current measurement in a motor speed control application. This amplifier is well suited for this application because of its high transient immunity (l0kV/µs). Its differential output feature is well suited to the differential input of the ADS7833. Keeping the signal transmission differential helps to preserve the high frequency noise rejection of the system.

A unique characteristic of the ISO130 is that it has a common mode output voltage of approximately 2.39V. To accept this level of CMV, the ADS7833 must be operated at a gain of 5V/V (±0.5V full scale differential input). (See Figure 3 and Table VII). Since the ISO130 has a gain of 8V/V, the maximum value of V_{SENSE} is 62.5mV. Thus, the value of R_{SENSE} is chosen to scale V_{SENSE} to this maximum value.

POWER-UP INITIALIZATION

When power is applied to the ADS7833, two conversion cycles are required for initialization and valid digital data is transmitted on the third cycle.

The first conversion after power is applied is performed with indeterminate configuration values in the double buffer output of the Input Setup Register. The second conversion cycle loads the desired values into the register. The third conversion uses those values to perform proper conversions and output valid digital data from each of the ADCs.

```
        movep    #>$0,x:$ffe4       ; Disable SAI transmit port
        movep    #>$0,x:$ffe1       ; Disable SAI receive port
        movep    #>$0,x:$fff1       ; Disable SHI port
        ;
        movep    #>$dfff00,x:$ffe5  ; Convert command
        movep    #>$101f00,x:$ffe6  ; DAC to midscale, G=1V/V, Channel 1 all ADCs
        movep    #>$0,x:$ffe7       ; For SS pin—enables SHI at proper time
        movep    #>$10d,x:$ffe0     ; Divide by 1 pre, divide by 13—96kHz conv @ 40MHz
        movep    #>$3,x:$ffe1       ; Enable SAI recv (rsng edge, MSB 1st, 16-bits, slave)

        movep    #>$2001,x:$fff0    ; Set narrow spike filter, CPOL=0, CPHA=1
        movep    #>$5,x:$fff1       ; Enable SHI (slave, no fifo, 16-bits)
        movep    #>$f,x:$ffe4       ; Enable SAI trans (rsng edge, MSB 1st, 16-bits, mstr)
        ;
wait    btst     #14,x:$ffe1        ; Look for a receive flag (left or right)
        jcs      data
        btst     #15,x:$ffe1
        jcc      wait
data    movep    x:$ffe2,x0         ; Get Sout1
        move     x0,x:$00           ; Save it
        movep    x:$ffe3,x0         ; Get Sout2
        move     x0,x:$01           ; Save it
        move     x:$fff3,x0         ; Get Sout3
        movep    x0,x:$02           ; Save it
```

TABLE VIII. Sample Code for Motorola DSP56004/7.

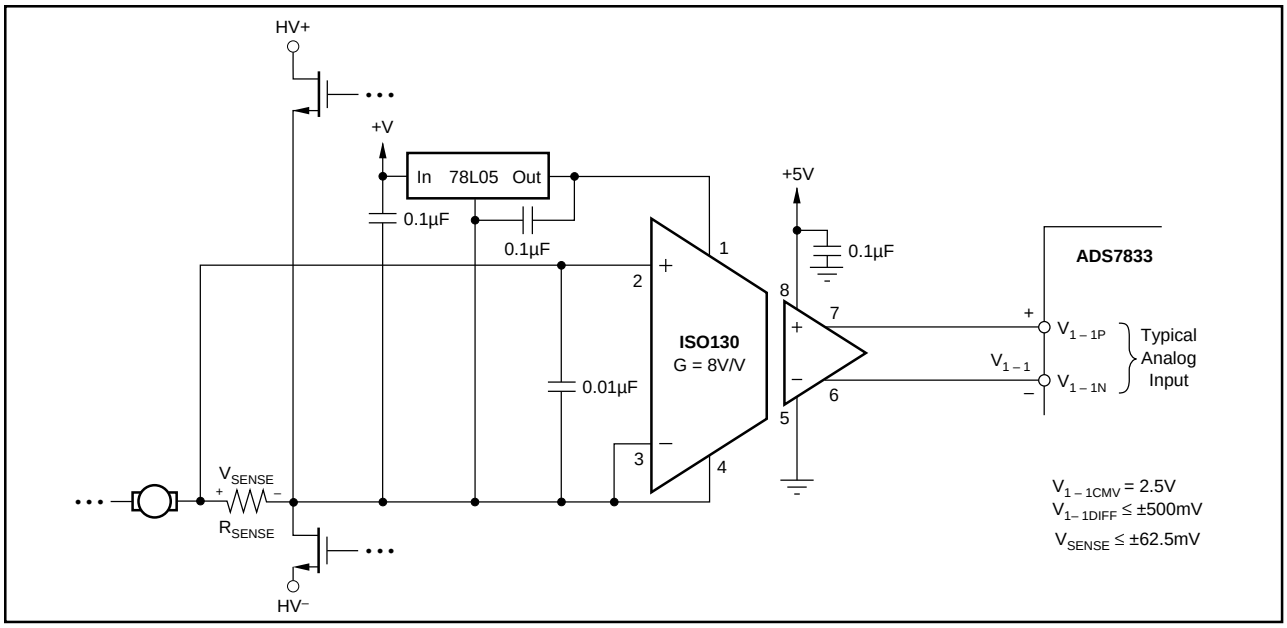


FIGURE 5. Typical Isolated Differential Analog Input.

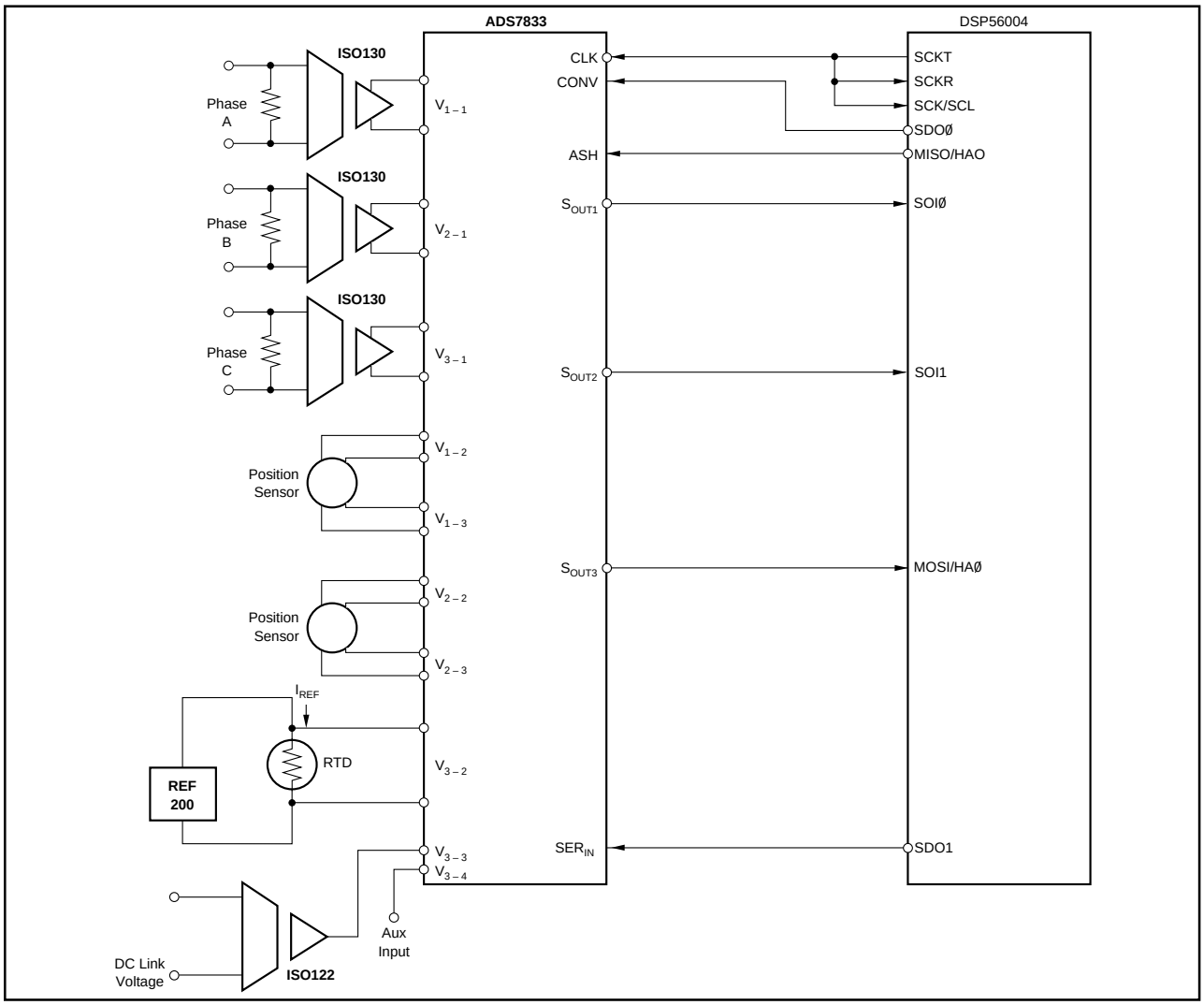


FIGURE 6. Motor Control Application Using Position Sensors.