

ADC601

12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

FEATURES

- FAST CONVERSION: 900ns
- CAN BE SHORT-CYCLED
- INPUT RANGES: $\pm 5V$, $\pm 10V$, 0 to $-10V$
- HIGH SIGNAL/NOISE RATIO: 68dB
- LOW IMD: 75dB
- PARALLEL AND SERIAL OUTPUT
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

The ADC601 is a high-speed Duolithic™ (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

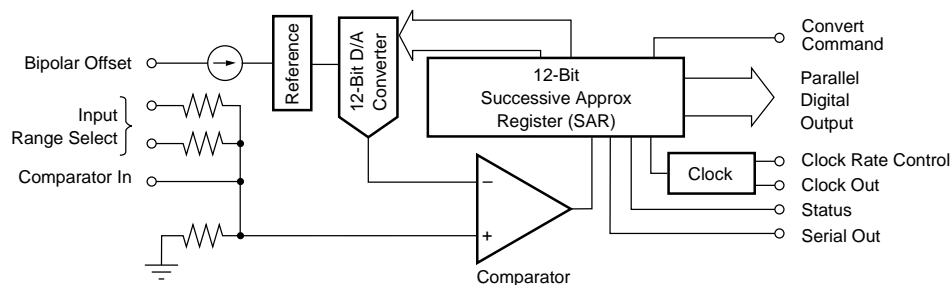
The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed

with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of $\pm 5V$, $\pm 10V$ and 0V to $-10V$. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are $\pm 15V$ and $+5V$.



Duolithic™ Burr-Brown Corporation

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, ±V_{CC} = ±15V, +V_{DD} = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

| PARAMETER | CONDITIONS | ADC601JG | | | ADC601KG | | | UNITS |
|---|--|----------|---|---|----------|-------------------|-----|--|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | | 12 | | | * | Bits |
| ANALOG CHARACTERISTICS | | | | | | | | |
| INPUTS | | | | | | | | |
| Voltage Ranges: Bipolar Unipolar Impedance: -10V to 0V, ±5V ±10V | Full Scale(FSR) ⁽¹⁾⁽²⁾ Full Scale(FSR) ⁽¹⁾⁽²⁾ | | ±5, ±10 0 to -10 1.4 2.4 | | | * | * | V V kΩ kΩ |
| TRANSFER CHARACTERISTICS | | | | | | | | |
| ACCURACY | | | | | | | | |
| Gain Error ⁽³⁾ Input Offset Error ⁽³⁾ : Unipolar Bipolar Integral Linearity Error Differential Linearity Error No Missing Codes Power Supply Rejection of Offset and Gain | 990ns Conversion Time 990ns Conversion Time 990ns Conversion Time 990ns Conversion Time 990ns Conversion Time Δ +V _{CC} = ±5% Δ -V _{CC} = ±5% Δ +V _{DD} = ±5% | | ±0.08 ±0.12 ±0.08 ±0.0036 ±0.0005 ±0.001 | ±0.55 ±1.2 ±0.8 ±0.024 ±0.024 Guaranteed | | * | * | % % of FSR % of FSR % of FSR % of FSR %FSR/%V _{CC} %FSR/%V _{CC} %FSR/%V _{DD} |
| DIGITAL CHARACTERISTICS | | | | | | | | |
| INPUT | | | | | | | | |
| Logic Family Convert Command Logic Voltages Convert Command Currents Convert Command | Logic Low Logic High Logic Low Logic High | 0 +2 | | TTL-Compatible CMOS +0.8 +V _{DD} -150 -150 High Level When Converting | | * | * | V V μA μA |
| CONVERSION TIME | | | | | | | | |
| Factory Set Power Supply Rejection of Conversion Time | Without User Adjustment D +V _{DD} = ±5% | | 0.9 ±1 | 1 | | * | * | μs ns/%V _{DD} |
| OUTPUT | | | | | | | | |
| Logic Family Bits 1 through 12, Serial, Status, Clock Out Internal Clock Frequency Status | Logic Low, I _{OL} = 3.2mA Logic High, I _{OH} = -1mA | +2.7 | | TTL-Compatible CMOS +0.1 +4.9 13 Low Level When Data Valid | | * | * | V V MHz |
| DYNAMIC CHARACTERISTICS ^{(4) (5) (6)} Tested using Sample/Hold Amplifier SHC804 and ADC601 (See Typical Performance Curves) | | | | | | | | |
| Differential Linearity Error | f _C = 10kHz: 68.3% of All Codes 99.7% of All Codes 100% of All Codes | | 0.5 0.8 1.0 | | | 0.4 0.6 0.7 | | LSB LSB LSB |
| Total Harmonic Distortion | f _C = 10kHz, f _S = 500kHz f _C = 10kHz, f _S = 1MHz f _C = 250kHz, f _S = 500kHz f _C = 500kHz, f _S = 1MHz | | -70 -74 -70 -68 | | | * | * | dBc dBc dBc dBc |
| Two-Tone Intermodulation Distortion ⁽⁷⁾ | f _C = 11kHz and 15kHz, f _S = 500kHz f _C = 50kHz and 55kHz, f _S = 500kHz f _C = 90kHz and 110kHz, f _S = 500kHz | | -79 -78 -77 | | | * | * | dBc dBc dBc |
| Signal-to-Noise and Distortion (SINAD) Ratio | f _C = 250kHz, f _S = 500kHz f _C = 500kHz, f _S = 1MHz | | 66 65 | | | * | * | dB dB |
| Signal-to-Noise Ratio (SNR) | f _C = 250kHz, f _S = 500kHz f _C = 500kHz, f _S = 1MHz | | 68 67 | | | * | * | dB dB |
| PERFORMANCE OVER TEMPERATURE | | | | | | | | |
| Gain Input Offset: Unipolar Bipolar Internal Linearity Error Differential Linearity Error No Missing Codes Conversion Drift | T _{MIN} to T _{MAX} T _{MIN} to T _{MAX} T _{MIN} to T _{MAX} 0.9μs Conversion Time T _{MIN} to T _{MAX} 0.9μs Conversion Time T _{MIN} to T _{MAX} 0.9μs Conversion Time T _{MIN} to T _{MAX} | | ±10 ±2 ±3 ±0.02 ±0.02 2 | ±30 ±7 ±10 Guaranteed | | * | * | ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C % of FSR % of FSR ns/°C |

SPECIFICATIONS (CONT)

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, ±V_{CC} = ±15V, +V_{DD} = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

| PARAMETER | CONDITIONS | ADC601JG | | | ADC601KG | | | UNITS |
|--|---|----------|-------|--------|----------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| POWER SUPPLY REQUIREMENTS | | | | | | | | |
| Supply Voltages: +V _{CC} | Nominal ±V _{CC} and +V _{DD} | +14.25 | +15 | +15.75 | * | * | * | V |
| -V _{CC} | | -14.25 | -15 | -15.75 | * | * | * | V |
| +V _{DD} | | +4.75 | +5 | +5.25 | * | * | * | V |
| Supply Currents: +I _{CC} | | 5.4 | 7.0 | | * | * | | mA |
| -I _{CC} | | -65 | -84.5 | | * | * | | mA |
| +I _{DD} | | 53 | 68.9 | | * | * | | mA |
| Power Consumption | | 1.3 | 1.7 | | * | * | | W |
| Thermal Resistance, θ _{JC} | | 25 | | | * | * | | °C/W |
| TEMPERATURE RANGE⁽⁸⁾ | | | | | | | | |
| Specification | | 0 | | +70 | * | | * | °C |
| Operating | | -25 | | +85 | * | | * | °C |

* Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB; f_c = input frequency; f_s = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. For example, unit connected for ±10V has 20V FSR. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board; with the test device in a (zero insertion force) socket. Thermal resistance will be lower if the ADC601 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

ABSOLUTE MAXIMUM RATINGS

| | |
|----------------------------|------------------|
| ±V _{CC} | ±18V |
| +V _{DD} | +7V |
| Digital Inputs | +5.5V |
| Analog Inputs | ±V _{CC} |
| Comparator Input | -3.7V to +0.7V |
| Case Temperature | +125°C |
| Junction Temperature | +165°C |
| Storage Temperature | -65°C to +150°C |

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

| | | | | |
|-------------------------------------|-------|--------|-----|---|
| Basic Model Number | _____ | ADC601 | () | G |
| Performance Grade Code | _____ | | | |
| J, K: 0°C to +70°C Case Temperature | | | | |
| Package Code | _____ | | | |
| G: Ceramic DIP | | | | |

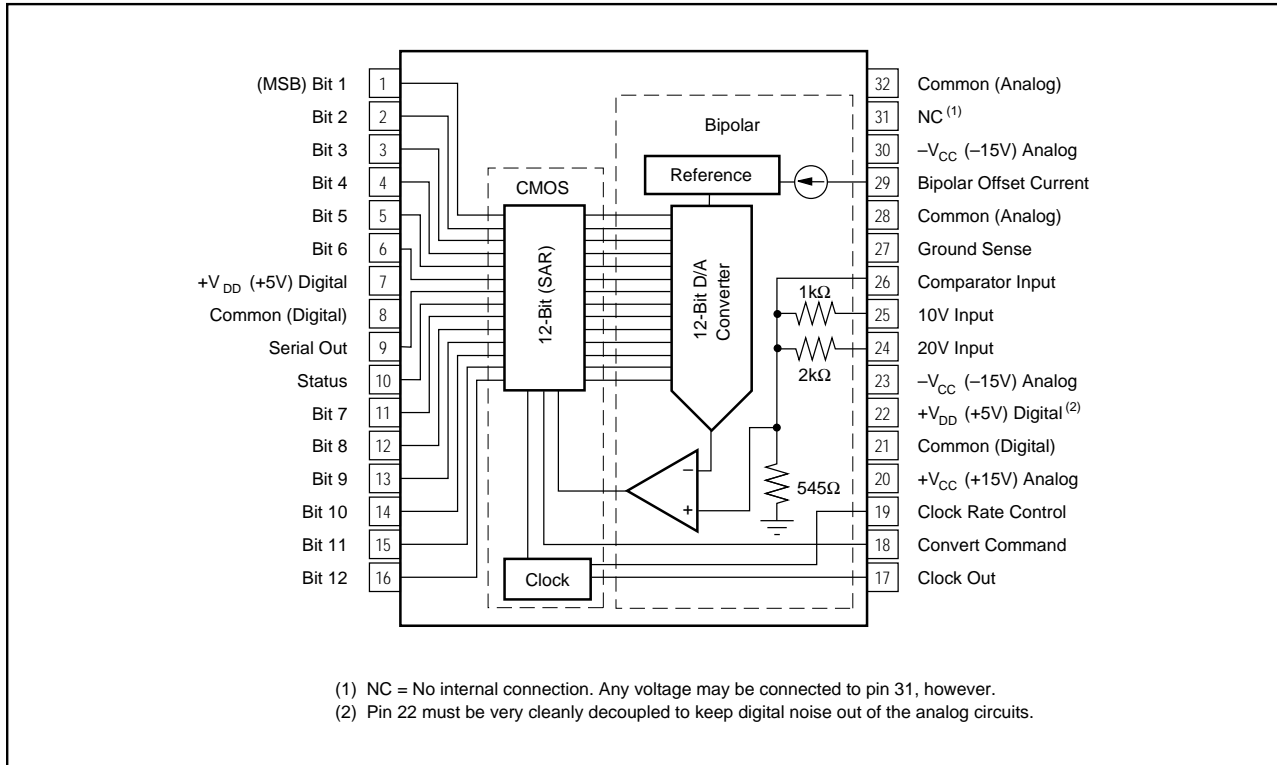
PACKAGE INFORMATION⁽¹⁾

| MODEL | PACKAGE | PACKAGE DRAWING NUMBER |
|----------|---------------------|------------------------|
| ADC601JG | 32-Pin Hermetic DIP | 172-2 |
| ADC601KG | 32-Pin Hermetic DIP | 172-2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



PIN DEFINITIONS

| PIN NUMBER | DESIGNATION | DESCRIPTION |
|---------------|------------------------|---|
| 1-6 and 11-16 | Bit 1 to Bit 12 | 12-bit parallel output data capable of sinking 3.2mA. |
| 9 | Serial Out | 12-bit serial data output synchronized with the negative edge of each appropriate clock cycle. |
| 10 | Status | Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t_{BBL} in the ADC601 timing diagram. |
| 17 | Clock Out | Negative edge indicates when serial data is valid. After convert command goes high, first cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command. |
| 18 | Convert Command | High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic. |
| 19 | Clock Rate Control | May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation. |
| 24 | 20V Input | 20V input range allows $\pm 10V_{p-p}$ analog input signal. Short to ground when not used. |
| 25 | 10V Input | 10V input range allows 0 to $-10V_{p-p}$ or $\pm 5V_{p-p}$ input range. |
| 26 | Comparator In | Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance. |
| 27 | Ground Sense | Ground Sense pin. (See text for use). |
| 29 | Bipolar Offset Current | Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation. |