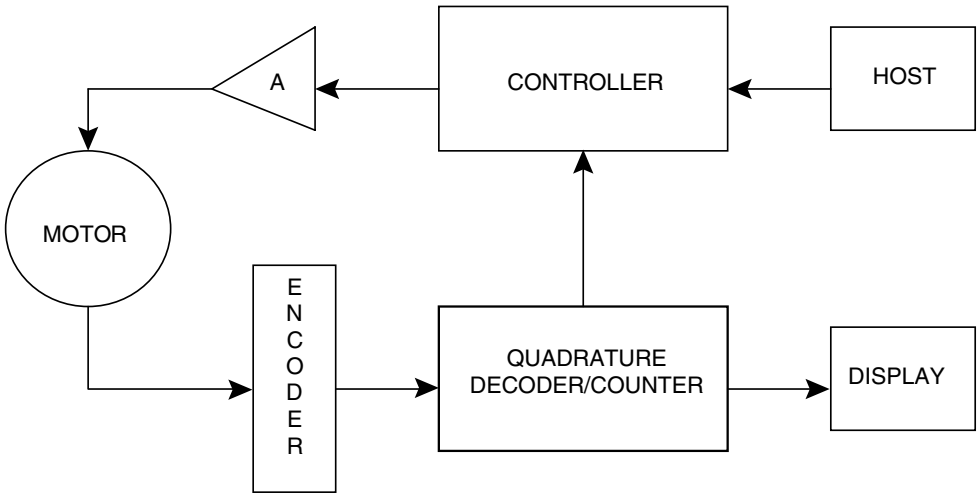
Quadrature Decoder/Counter using Atmel FPGA/FPSLIC™

The purpose of a quadrature decoder/counter is to take some of the real-time computational load off the microprocessor. When the processor reads the output signals of the position encoder, every change in state must be detected. This means that for an encoder of 250 pulse per channel per revolution turning at a modest 6000 rpm, the processor must detect and decode 100,000 state changes per second. This is difficult for most microcontrollers, and many systems use higher speeds and/or even denser encoders.

The solution to this difficulty is a circuit that will detect each of these state changes and send them to a counter. Each time a state change is detected in the positive direction, the decoder will increment the counter; a change in the other direction causes the counter to be decremented. Thus the counter will keep a running count of how far the encoder has moved, until it overflows. Now the microprocessor can read the number in the counter and compare that number to a previous reading in order to measure the distance traveled. Since the counter stores the position changes, a system using an 8-bit counter can measure the position from signals whose frequency is about 127 times higher than that of the fastest signals that can be measured by a software-only system. In a similar way, the 4-bit counter can read signals approximately 8 times faster than those read only by software.

Figure 1. Typical Application Block Diagram



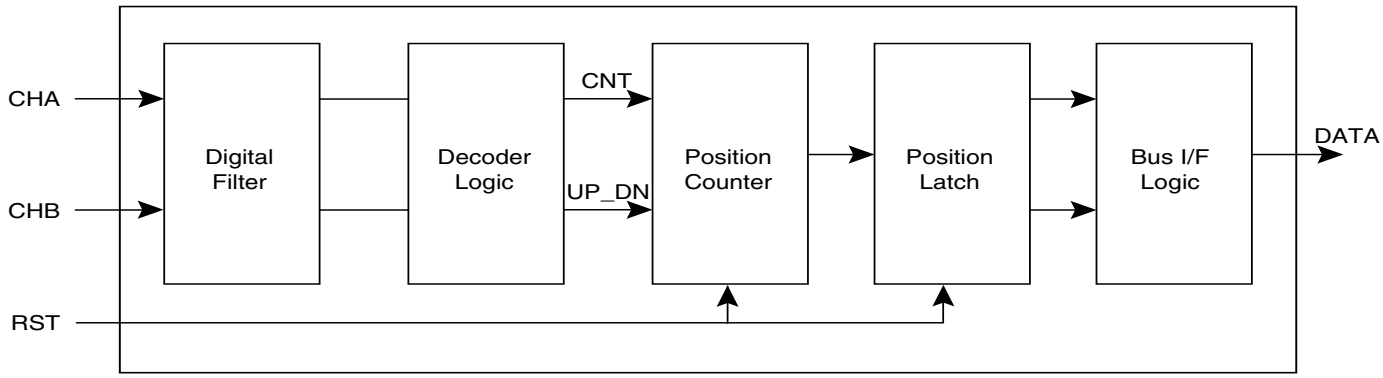
Programmable SLI
AT40K
AT94K

Application Note

Rev. 3037A–FPSLI–04/02

Functional Description

Figure 2. Quadrature Decoder/Counter Block Diagram



Functional Pin Description

Pin	Description
CLK	System Clock
CHA CHB	CHA and CHB are inputs that accept outputs from a quadrature-encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase.
RST	Asynchronous active low reset signal that clears the internal position counter and position latch.
OE	Active-low output enable input signal
SEL	The input controls the data byte from the position latch. “0” selects high byte and “1” selects lower byte.
CNT	Pulse generated from the decoder when the quadrature decoder has detected a state transition.
UP_DN	Output from the quadrature decoder. This signal will determine whether the counter is counting up or down.
DATA	Output databus

Digital Filter

The digital filter is responsible for rejecting noise on the incoming quadrature signals. This is achieved by combining Schmitt triggered inputs and three clock-cycle delay filters. This combination rejects low level noise and large, short duration noise spikes that typically occur in motor system applications.

The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. By this method the short noise spikes between rising clock edges are ignored and pulses shorter than two-clock period are rejected.

Decoder Logic

The decoder logic decodes the incoming filtered signals into count information. The decoder samples the outputs of channels A and B. Based on the past binary state of the two signals and the present state, it outputs a count signal (CNT) and direction signal (UP_DN) to the position counter, see Figure 3. Channel A leading Channel B results in counting up. Channel B leading channel A results in counting down.

Figure 3. Counter State Transition Diagram

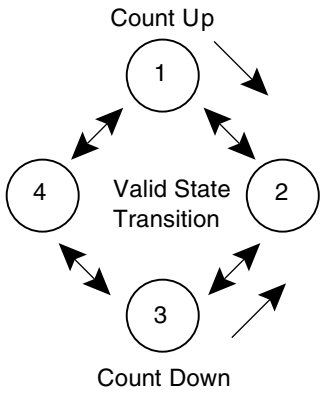


Table 1. Count Signal Values

CHA	CHB	UP_DN
1	0	1
–	1	0

For better system control and improved resolutions, the designer can multiply the resolution of the incoming signals by a factor of four (4 x decoding).

Position Counter

The binary up/down counter counts on rising clock edge. Channel A leading channel B results in counting up. Channel B leading Channel A results in count down.

Position Data Latch

The position data latch captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic during two-byte operation. The inhibit logic samples the OE and SEL control signals and does the conditional inhibit of the position data register.

Table 2. Position Data Latch

SEL	OE	CLK	INH	Action
L	L	H-L	H	Read High Byte
H	L	H-L	H	Read Low Byte
X	H	X	0	Output Tri-state

Bus I/F Logic

Consists of multiplexers and tri-state output buffer. This allows the independent access to the low and high bytes of the position data latch.

Design Implementation

A simple two-channel quadrature decoder/counter is implemented using VHDL®. The design involves two-channel digital filter, quadrature decoder, 16-bit position counter, 16-bit position latch and 8-bit bus interface logic.

The design is successfully fitted into Atmel AT40K05 and it requires 87 core cells and 17 I/Os.

Tools Used

Synthesis: Exemplar™'s LeonardoSpectrum™ version: v20001b_atmel.106

FPGA Place and Route: Atmel IDS7.5 (with level 1 patch)

Simulation: Model Technology™ ModelSim® simulator.

The source files for this application note can be found in the FPSLIC Software section of the Atmel web site (http://www.atmel.com), under the **3037.zip** archive.

The contents of the zip file are shown in Table 1.

Table 1. 3037.zip Contents

File	Description
Quad_top.vhd	Top quadrature module
Digital_filter.vhd	Two-channel Digital Filter
Quad_decoder.vhd	1X quadrature decoder
Position_counter.vhd	16-bit position counter
Position _latch.vhd	16-bit position latch and 8-bit bus interface logic

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