Testing the ATSTK94

This tutorial shows the user how to test the ATSTK94 Board. The following example uses a sample bit stream file supplied with the kit to perform a board test. It is recommended to perform the board test when you receive the kit to test both your connections to the board and the board itself.

The main steps in this tutorial are:

- Programming the Configurator (AT17XX) with a Bit Stream File
- Downloading the Configuration Data to the AT94K FPSLIC[™] Device During Power Up.

Setting up the Example Files

In this tutorial all paths are given assuming a default install of c:\SystemDesigner. If you have installed System Designer[™] in another drive or directory, remember to change the path to your actual System Designer directory.:

- 1. Install System Designer from the CD, please refer to the "System Designer User Guide" available on the Atmel web site, at http://wwww.atmel.com/dyn/products/tools_card.asp?tool_id=2752.
- 2. Request and Configure your license.
- 3. Install CPS from the System Designer CD.
- 4. Copy the test_fpslic.bst file from c:\SystemDesigner\Examples\at94k\ATSTK94 Designs or from http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2750.

Setting up the Hardware

- 1. Connect the 25-pin parallel cable to the 25-pin male connector of the ATDH2225 download cable. The 10-pin female header plugs into the 10-pin male header (J1) on the ATDH94STKB board.
- 2. Connect the power supply from an AC outlet to the 9V DC connector (P3) on the ATSTK94 board.
- Make sure to set the jumpers located between the LEDs and Switches appropriately. LED1 to LED8 should be connected to AVR side. Switches SW1 to SW4 should be connected to AVR side, and switches SW5 to SW8 should be connected to FPGA side.
- 4. Adjust *SW10* to the *PROG* position and *SW14* to the *ON* position. The power LED lights.



ATST94K

Tutorial

Rev. 2449B-FPSLI-03/03





Downloading to the Configurator

1. Go to the *Start* menu and choose *Programs > Atmel > Atmel CPS 8.0x*. Atmel CPS opens, see Figure 1.

Figure 1. Atmel CPS Window

ile Calibrate <u>H</u> elp	URATUR PRUGRAMMING STSTEM	
Procedure: /P: Partitie Files Input File: C:\training Output File: C:\training Checksum: Checksum: Checksu	rr, program and verify from an Atmel file Info One or more Atmel (bst) files subsequent download session checksum can be obtained f each programming session. In HEX values are only append files which have been partitic must be of the form <file>.bst COMM Port: LPT1 w ▼ Data Rate: Fast 40K/AT94K ▼ A2 Bit Levet: Low</file>	may be generated for ons. The optional rom the log output of n this version of CPS, led to the .BST output oned. The output file t.
	Start Procedure Restore Defaults	View Log File

- 2. Select /P Partition, Program and Verify from an Atmel File from the Procedure pull-down menu in the CPS window.
- 3. Use the _____ button from the *Input File* pull-down menu to locate the test_fpslic.bst file under c:\training\fpslic\lab1.
- 4. Use the ____ button from the *Output File* pull-down menu to indicate the out.bst file under c:\training\fpslic\lab1.
- 5. Select 1M from the EEPROM Density pull-down menu.
- 6. Use the default options for the rest.
- 7. Press Start Procedure to program the Configurator.

If the utility has not been calibrated on a given PC, the Clock Calibration dialog will be displayed when the *Start Procedure* button is clicked, see Figure 2. For best results, it is highly recommended to allow *Clock Calibration* to proceed prior to the execution of the procedure. The clock calibration routine accounts for any variations in time delay units between different processors.





8. Press Yes. A calibration accuracy dialog box opens.

Low, Medium and *High* refer to the accuracy of the calibration. A high level of calibration will require more time to complete. Calibration can be performed again or at a later time by going to the *Calibrate* menu and selecting *Calibrate now*. The out.bst file can be overwritten.

If successful, the results are shown in Figure 3.

ATMEL AT17 CONFIGURATOR PROGRAMMING S	YSTEM _ 🗖 🗙	
<u>Fi</u> le Calibrate <u>H</u> elp		
Procedure: /P: Partition, program and verify from an Atme Files Input File: C:\training\fpslic\lab1\test_fpslic. Implies Output File: C:\training\fpslic\lab1\out.bst Implies Checksum: 1884688 Options EEPROM Density: 1M Reset Polarity: Low Implies AT 10% (AT 04% Implies)	Info One or more Atmel (.bst) files may be generated for subsequent download sessions. The optional checksum can be obtained from the log output of each programming session. In this version of CPS, HEX values are only appended to the .BST output files which have been partitioned. The output file must be of the form <file>.bst. COMM Port: Data Rate: Fast</file>	
FPGA Family:	A2 Bit Level: Low	
Console Sum of device bytes: 1884688 Setting reset polarity to Low : Reset Handling for High Density Devices Device data (46555 bytes) has been written to file c:\training\fpslic\lab1\out.bst. Verifying AT17Cxxx contents The Procedure Completed 46555 bytes of 46555 total bytes successfully verified SUMMARY: Number of Warnings: 0 Number of Fatal Errors : 0 Normal program completion		
Start Pr	ocedure Restore Defaults View Log File	

- 9. After CPS reports successful completion you can switch from Prog. to Run.
 - Your design starts to run. The Alphanumeric will show a count sequence from 0 to 9 and from A to Z and will then reset to 0. The LED will show the counting up sequence. If your design does not run immediately you can set *JP19* to *RESET* and use the *RESET* button *SW12* to force a download from the Configurator to the FPSLIC device. You can also power-cycle the device.





The Checksum number is the number of data bits in the bitstream file, the checksum number shown here is for test_fpslic.bst file. This number can be used to check if the data is corrupted during file transfer.

Your design can encounter the following errors:

Hardware Troubleshooting

Error message "Expected 1 but found 0"

- No Power to the board
- Prog/ Run in the wrong position

or:

FATAL_ERROR: CMD ack_sense timed out Double check the orientation of cable connected to evaluation board

Any other failure would be related to the following:

- Check to see that the Jumpers and Switches are in default positions, see Table 1.
- The next area to check is the pinlocks. In Figaro, during the parts process, make sure that you have selected to assign pinlocks. Without performing this step, your project will not run on the board, since you have not connected the signals to the correct pins on the board.
- Check to see that the AVR-FPGA Interface has the correct connections.
- Run co-verification on your design

Please refer to the CPS Troubleshooting guide for a complete description. Go to the *Help* menu and select *Contents > Trouble Shooting.*

Jumper/Switch	Default Position
JP 1-16	The default position for all the switches and LEDs is with the Jumper set to the "A" position, which means that the switches and LEDs are connected to the microcontroller. By setting the jumpers to the "F" position, the switches and LEDs are connected to FPGA.
JP17	Rev 2 – The jumper is set towards the edge of the board, this connects to the 4 MHz crystal. Connecting to other side will connect to the 18 MHz crystal. Rev3 and beyond – The position of the jumper is changed and it should be set on the inner side to connect to the 4 MHz crystal. Connecting towards the outer side of the board will connect to the 18 MHz crystal.
JP18	Has a Jumper Connected
JP19	Set to the RESET Position
JP20	Jumper connects the SER_EN pin of the AT17 device to the PORTE pin 7 of the microcontroller. By connecting this jumper, you can perform 2-wire serial interface. Default is "Not Connected"
JP21	Jumper Connects CEO/A2 to V _{CC} . Default is "Not Connected"
JP22	Jumper connects the write protect pins of the AT17 device to $V_{\rm CC}. \mbox{Default}$ is "Not Connected"
JP23	Rev4 and beyond – Jumper connects the write protect pins of the AT17 device to $V_{\text{CC}}.$ Default is "Not Connected"
ON/OFF (Sw14)	Power Switch. Default Position Off
Run /Prog	Switch Set to Prog.

 Table 1. Default for Jumpers and Switches





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