
IP Core Generator: Shift Register

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Input Type Selection
- Output Type Selection
- Variable Width of Shift Register
- Optional Enable
- Clock Inversion Capability
- Initialization Polarity Selection
- Initialization Selection
- Preset and Parallel Input Radix Selection

Description

The Shift-register generator can be used to create serial, serial-parallel, parallel-serial and parallel-parallel shift registers.



**Programmable
SLI
AT40K
AT40KAL
AT94K**

**Application
Note**

Rev. 2446A-12/01



Parameters

Parameter	Value	Explanation
Input Type	Serial	Input is serial
	Parallel (Variable)	Input is parallel
	Parallel (Constant)	Input is parallel, with a fixed value
Output Type	Serial	Output is serial
	Parallel	Output is parallel
Width	Integer > 0	Width of shift register
Enable	Boolean	Add an enable pin to the register
Invert Clock	Boolean	Invert the clock input
Initialization polarity = Low	Boolean	Reset/set/preset input is active low
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are reset automatically on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Preset and Parallel Input Radix	Binary	Preset and parallel input values are specified using binary representation
	Octal	Values are specified in octal
	Decimal	Values are specified in decimal
	Hex	Values are specified in hexadecimal

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	Yes	Data input for parallel-input shift registers
In	SHIFTIN	Yes	Data input for serial-input shift registers
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	ENABLE	Yes	Register enable input
In	SHIFTEN	Yes ⁽¹⁾	0 = load data in 1 = shift
In	R/RN/S/SN/P/PN	No	Reset/set/preset (active high/low)
Out	Q[Width - 1:0]	Yes	Data output for parallel-output shift registers
Out	SHIFTOUT	Yes	Data output for serial-output shift registers

Note: 1. With parallel input

Truth Table⁽¹⁾

Input						Output	
RN	DATA[W - 1:0]	CLK	ENABLE	SHIFTIN	SHIFTEN	Q[W - 1:0]	SHIFTOUT
0	X	X	X	X	X	0	Q(N - 1)
1	X	0 > 1	X	X	X	No Change	Q(N - 1)
1	0	0 > 1	1	X	1	0	Q(N - 1)
1	1	0 > 1	1	X	1	1	Q(N - 1)
1	X	0 > 1	1	SI	0	$Q(i) = Q-(i - 1)$ ⁽²⁾ $Q(0) = SI$	Q(N - 2)

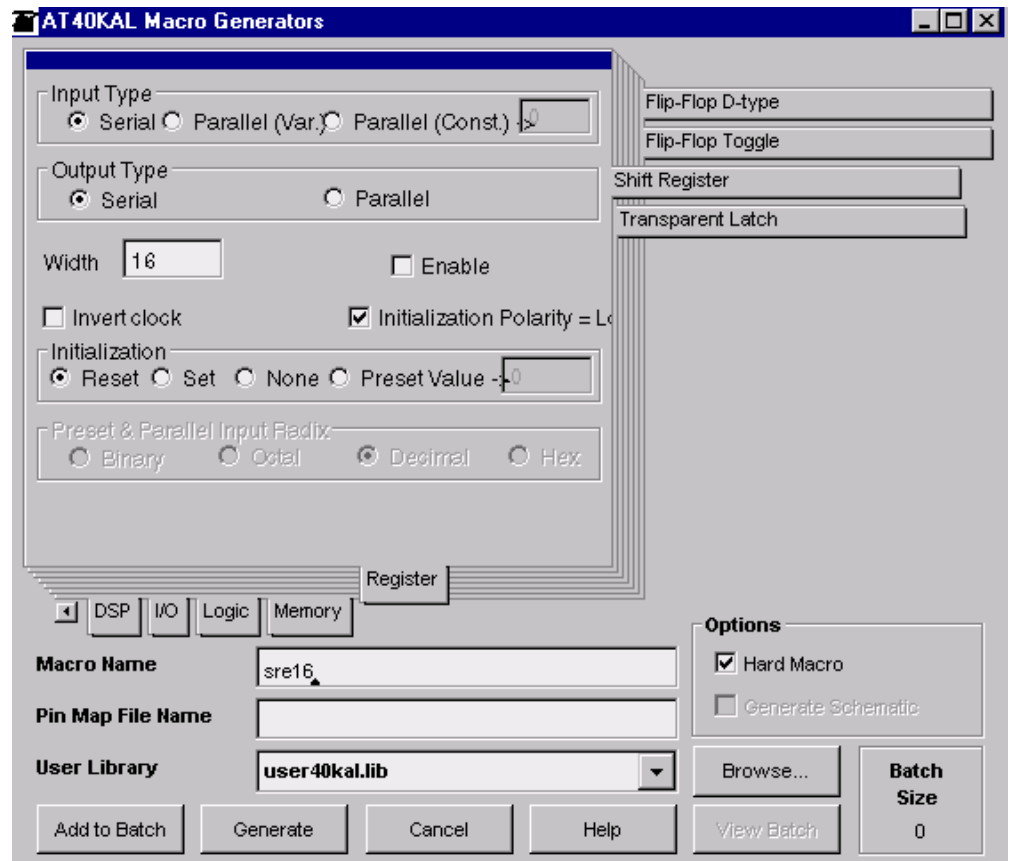
- Notes:
1. This truth table assumes that an active-low reset and non-inverted clock have been selected.
 2. Q - i is the value of Q preceding the clock transition.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	sre16	226.2	4.4	16	1 x 16
AT40K	sre8	226.2	4.4	8	1 x 8
AT94K/ AT40KAL	sre16	598.8	1.7	16	1 x 16
AT94K/ AT40KAL	sre8	598.8	1.7	8	1 x 8

Figure 1 shows an example of the sre16 macro options.

Figure 1. Shift Register





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