

IP Core Generator: Mux

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Variable Number of Parallel Muxes
- Variable Number of Inputs per Mux

Description

The Mux generator can be used to generate one or more muxes controlled by a single SELECT bus input. The width of each Mux is user programmable.

Parameters

Parameter	Value	Explanation
Number of Muxes	Integer ≥ 1	Number of parallel mux components in the macro
Number of Inputs per Mux	Integer ≥ 1	Number of inputs that each mux switches

Pins⁽¹⁾

Type	Name	Option	Explanation
In	S[log2 (Width) - 1:0]	No	Mux select pins, Log2-bits wide
In	DATA[Size - 1:0]	No	Mux input pins
Out	RESULT[Size - 1:0]	No	Mux output

Note: 1. Size represents the number of muxes and Width is the number of inputs to each mux.



**Programmable
SLI
AT40K
AT40KAL
AT94K**

**Application
Note**



Truth Table

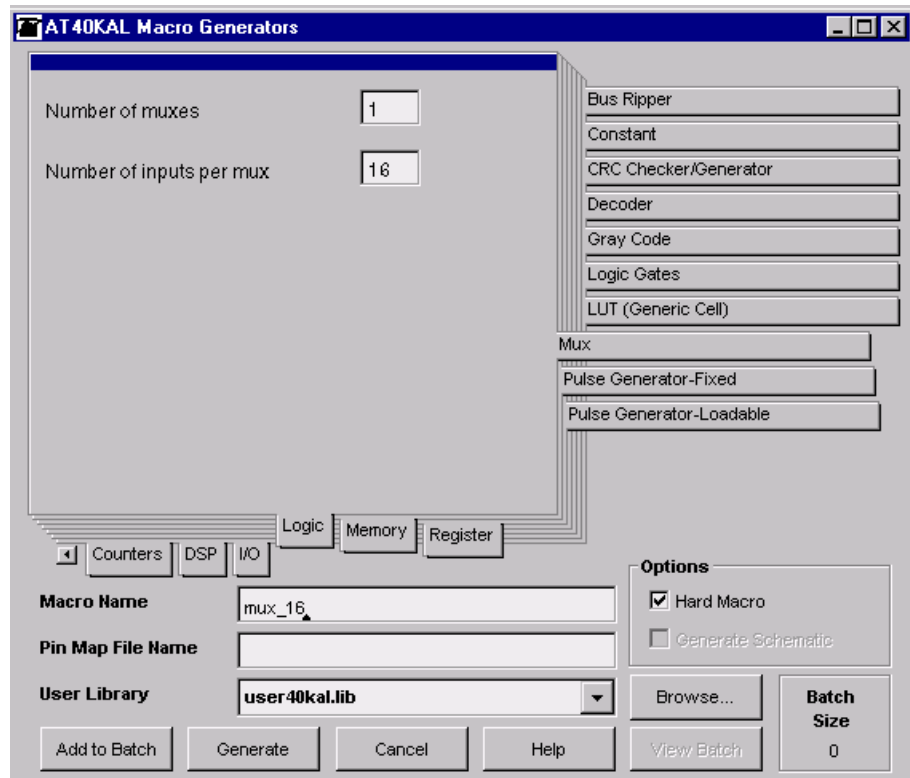
Input		Output
S	DATA	RESULT
0	..XXX0	0
0	..XXX1	1
1	..XX0X	0
1	..XX1X	1
2	..X0XX	0
2	..X1XX	1
.		.
.		.
.		.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	mux_16	127.1	7.9	16	8 x 2
AT40K	mux_8	130.5	7.7	8	4 x 2
AT94K/ AT40KAL	mux_16	140.6	7.1	16	8 x 2
AT94K/ AT40KAL	mux_8	154.1	6.5	8	4 x 2

Figure 1 shows an example of the mux_16 macro options.

Figure 1. Mux Generator





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