IP Core Generator: Bus Ripper

Features

- Accessible from the Macro Generator Dialog and HDLPlanner[™] Included in IDS for FPGA Devices and System Designer[™] for AT94K FPSLIC[™] Devices
- Variable Width of Input Bus
- Used for Schematic Designs Only

Bus Ripper

The Bus Ripper generator allows the user to produce variable-width "soft" buffers for re-naming buses within a design. When the design is imported into IDS, the mapping tools will identify the bus ripper macro as redundant logic and remove it from the netlist. The bus rippers are a fast and convenient method of re-labeling buses in a design without consuming unnecessary logic resources in the final implementation.

Note: Ensure that Mapping is enabled when importing a circuit containing bus ripper macros, to prevent extra logic from being added to the design. From the **Options** menu, select **Options** and then **Mapping**. The **Mapping Enabled** option should be checked.

Parameters

Parameter	Value	Explanation
Width	Integer	Width of input bus

Pins

Туре	Name	Option	Explanation
In	INPUT[Width - 1:0]	No	Input bus
In	OUTPUT[Width - 1:0]	No	Output bus

Figure 1 shows an example of the bsr16 macro options.



Programmable SLI AT40K AT40KAL AT94K

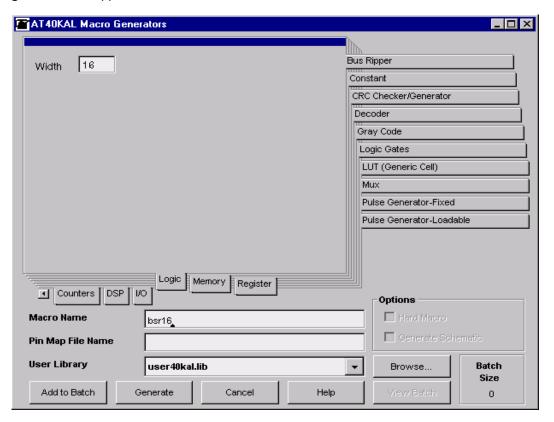
Application Note







Figure 1. Bus Ripper Generator





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