IP Core Generator: I/O Buffer

Features

- Bi-directional I/O Buffer
- Input I/O Buffer
- Output I/O Buffer
- Accessible from the Macro Generator Dialog and HDLPlanner[™] Included in IDS for FPGA Devices and System Designer[™] for AT94K FPSLIC[™] Devices
- Select TTL or CMOS Threshold on Inputs
- Optional Extra Delay on Inputs
- Optional Schmitt Trigger on Inputs
- Variable Slew Rate on Outputs
- Select Enable, Open Source or Open Drain on Outputs
- Optional Pull-up or Pull-down Resistors
- Variable Width
- Used Only with Schematic Designs

Bi-directional I/O Buffer

The bi-directional I/O buffer generator can be used to generate a soft macro (schematic only) which uses the specified options. This macro is not stored in the library, but becomes a part of the design. It generates a schematic symbol that can be used for blocks of I/O to simplify schematics. The generator provides a simple means for connecting I/Os to buses within the design. It also facilitates I/O selection as all of the parameters can be specified and the program will choose the appropriate cell from the library.



Programmable SLI AT40K AT40KAL AT94K

Application Note

Rev. 2426B-1/02





Parameters

Parameter	Value	Explanation
loout Threehold	TTL	The input threshold is TTL compatible
input i nresnoid	CMOS	The input threshold is CMOS compatible
	0	The input has no additional delay associated with it
Input Extra Dalay (na)	1	The input has an extra delay of approximately 1 ns
Input Extra Delay (IIS)	3	The input has an extra delay of approximately 3 ns
	5	The input has an extra delay of approximately 5 ns
Input Schmitt Triggering	Boolean	The input Schmitt trigger circuit is enabled
	Fast	The output buffer has fast drive (maximum slew rate)
Output Slewrate	Medium	The output buffer has medium drive (medium slew rate)
	Slow	The output buffer has standard drive (reduced slew rate)
	Enable	The output has an enable pin
Output Type	Open Source	The output is an open source
	Open Drain	The output is an open drain
	None	Pad pins have no pull-up or pull-down resistor
Pull Resistor	Pull Up	Pad pins have pull-up resistor
	Pull Down	Pad pins have pull-down resistor
Width	Integer > 0	Width of input and output data

Pins

Туре	Name	Option	Explanation
In	A[Width - 1:0]	No	Data input from the core to the I/O
In	OE[Width - 1:0]	Yes	Output enable input from the core to the I/O
In/Out	PAD[Width - 1:0]	No	Pad pin of I/O (bi-directional)
Out	Q[Width - 1:0]	No	Output from the I/O to the core

The following user configurable memory bits, which are set depending on the previous page selection of parameters, provide control of the I/O logic.

- TTL/CMOS Inputs: A user configurable bit determining the threshold level (TTL or CMOS) of the input buffer.
- Schmitt Triggering: A user configurable bit determining whether a Schmitt trigger circuit on the input pad should be enabled or disabled. The Schmitt trigger is a regenerative comparator circuit, which improves the rise and fall times (leading and trailing edges) of the incoming signal.
- Extra Delay: The input buffer can have four different intrinsic delays. This lets the user specify an extra delay on the input signal in order to meet any data-held requirements. A value of "0" means no extra delay above the intrinsic delay of the input buffer. Delays of approximately 1, 3 and 5 ns can also be set.
- Open Source/Open Drain/Tri-state Outputs: User configurable bits that set the output drive to either tri-state, open source (1 or Z) or open drain (0 or Z).
- Slew Rate Control: User configurable bits that control the output drive. When set to "FAST", the output buffer has full drive capability 20-mA buffer. The "MEDIUM" setting produces a medium-drive 14-mA buffer, while "SLOW" gives a standarddrive 6-mA buffer.
- Pull-up/Pull-down: User configurable bits controlling the pull-up and pull-down transistors in the I/O pin. These supply either a weak "1" or a weak "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

Figure 1 shows an example of the bid16 macro options.

AT40KAL Macro 6	ienerators				_ 🗆
Register None O	Input O Ou	tput O Both	BiDi	rectional I/O Buffer ut I/O Buffer]
🔲 Invert i/p Clod	Invert o/p Clock	Initialization Po	larity=Low	tput I/O Buffer	
Input Extra Delay	(ns) 1 O	3 0 5			
Input Schmitt trig Output Slewrate	ggering Width	16			
 Fast 	C Medium	O Slow			
Output Type Enable	O Open S	ource O Oper	n Drain		
Pull Resistor None	O Pull Up	O Pull	Down		
	Counters DSP		Dry Register	Options	
Macro Name	bid16			Hard Macro	
Pin Map File Name				Generate Sc	hematic
loor Library	user40ka	.lib	•	Browse	Batch
USEL LIDEALY				•	Sizo

Figure 1. Bi-directional I/O Buffer Generator





Input I/O Buffer

The input I/O buffer generator can be used to generate a soft macro (schematic only) which uses the specified options. This macro is not stored in the library, but becomes a part of the design. The generator provides a simple means for connecting I/Os to buses within the design. It also facilitates I/O selection as all of the parameters can be specified and the program will choose the appropriate cell from the library.

Parameters

Parameter	Value	Explanation		
Threaded	TTL	Input threshold is TTL compatible		
Threshold	CMOS	Input threshold is CMOS compatible		
Width	Integer > 0	Width of input and output data		
	0	The input has no additional delay associated with it		
Extra Dolov	1	The input has an extra delay of approximately 1 ns		
Extra Delay	3	The input has an extra delay of approximately 3 ns		
	5	The input has an extra delay of approximately 5 ns		
	None	Pad pins have no pull-up or pull-down resistor		
Pull Resistor	Pull-up	Pad pins have pull-up resistor		
	Pull-down	Pad pins have pull-down resistor		
Schmitt Triggering	Boolean	The input Schmitt trigger circuit is enabled		

Pins

Туре	Name	Option	Explanation
In	PAD[Width - 1:0]	No	Data input to the chip (pad pin)
Out	Q[Width - 1:0]	No	Output from the I/O to the core

The following user configurable memory bits, which are set depending on the above selection of parameters, provide control of the I/O logic.

- TTL/CMOS Inputs: A user configurable bit determining the threshold level (TTL or CMOS) of the input buffer.
- Schmitt Triggering: A user configurable bit determining whether a Schmitt trigger circuit on the input pad should be enabled or disabled. The Schmitt trigger is a regenerative comparator circuit, which improves the rise and fall times (leading and trailing edges) of the incoming signal.
- Extra Delay: The input buffer can have four different intrinsic delays. This lets the user specify an extra delay on the input signal in order to meet any data hold requirements. A value of "0" means no extra delay above the intrinsic delay of the input buffer. Delays of approximately 1, 3 and 5 ns can also be set.
- Pull-up/Pull-down: User configurable bits controlling the pull-up and pull-down transistors in the I/O pin. These supply either a weak "1" or a weak "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

Figure 2 shows an example of the iib16 macro options.

AT40KAL Macro Generators		_ 🗆 ×
■ Register IO ■ Inverticlock ■ Initialization Polarity = Low	BiDirectional I/O Buffer	·]
Width 0	Output I/O Buffer	
Extra Delay (ns) © 0 0 1 0 3 0 5 Pull Besistor		
O None O Pull Up Pull Down		
Schmitt triggering		
	Options	
Macro Name iib16	Hard Macro	
Pin Map File Name	Generate Sch	rematic
User Library user 40kal.lib	▼ Browse	Batch
Add to Batch Generate Cancel Help	View Batch	0

Figure 2. Input I/O Buffer Generator





Output I/O Buffer

The output I/O buffer generator can be used to generate a soft macro (schematic only) which uses the specified options. This macro is not stored in the library, but becomes a part of the design. The generator provides a simple means for connecting I/Os to buses within the design. It also facilitates I/O selection as all of the parameters can be specified and the program will choose the appropriate cell from the library.

Parameters

Parameter	Value	Explanation		
	Normal	The output has no enable pin		
	Enable	The output has an enable pin		
Туре	Open Source	The output is an open source		
	Open Drain	The output is an open drain		
Width	Integer > 0	Width of output data		
	Fast	The output buffer should be fast drive (maximum slew rate)		
Slewrate	Medium	The output buffer should be medium drive (medium slew rate)		
	Slow	The output buffer should be standard drive (reduced slew rate)		
	None	Pad pins have no pull-up or pull-down resistor		
Pull Resistor	Pull-up	Pad pins have pull-up resistor		
	Pull-down	Pad pins have pull-down resistor		

Pins

Туре	Name	Option	Explanation
In	A[Width - 1:0]	No	Data input from the chip
In	OE[Width - 1:0]	Yes	Tri-state enable pins
Out	PAD[Width - 1:0]	No	Output from the I/O (pad pin)

The following user configurable memory bits, which are set depending on the above selection of parameters, provide control of the I/O logic.

- Open Source/Open drain/Tri-state Outputs: User configurable bits that set the output drive to either tri-state, open source (1 or Z) or open drain (0 or Z).
- Slew Rate Control: User configurable bits that control the output drive. When set to "FAST", the output buffer has full drive capability 20-mA buffer. The "MEDIUM" setting produces a medium-drive 14-mA buffer, while "SLOW" gives a standarddrive 6-mA buffer.
- Pull-up/Pull-down: User configurable bits controlling the pull-up and pull-down transistors in the I/O pin. These supply either a weak "1" or a weak "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

Figure 3 shows an example of the oib16 macro options.

AT40KAL Macro Ge	enerators				
Type	abla 🔿 Onan Sa	urca <mark>O</mark> , Onan D	min	BiDirectional I/O Buffer	
	iable o openioc			nput I/O Buffer	
🔲 Register IO 🗌 Inv	ert Clock 🔽 Initial	ization Polarity	Out;	out I/O Buffer	
Width 16					
Slewrate Fast	O Medium	O Slow			
Pull Resistor None	O Pull Up	O Pull Do	wn		
		b			
CacheLogic C			Y Register	_ Options	
Macro Name	oib16			Hard Macro	
Pin Map File Name				🗌 Generate Sch	ematic
User Library	user40kal.lib		•	Browse	Batch
,					SIZE

Figure 3. Output I/O Buffer Generator





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