Implementing FreeRAM[™] inside the FPGA or AT94K Series FPSLIC[™] Using VHDL with IP Core Generator

Features

- Generating the RAM Component Using the IDS Macro Generator
- Checking the Design with Simulation
- Creating a New Library
- Using IP Core Generator
- Switchable for AT40K, AT40KAL and AT94K

Introduction

The purpose of this application note is to inform users of how to use VHDL with IP Core Generator to implement the FreeRAM inside the AT40K Field Programmable Gate Array (FPGA) for the AT94K Field Programmable System Level Integrated Circuit (FPSLIC).

testram.vhd and testram_test_bench.vhd are required for this example. These files can be found under C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram.

Note: This particular example describes how to implement a 32 x 4 asynchronous dual-port RAM cell in your VHDL file using LeonardoSpectrum[™].



Programmable SLI AT40K AT40KAL AT94K

Application Note

Rev. 2298A-08/01





Generate the RAM Component Using the IDS Macro Generator

- 1. Open Figaro IDS.
- Launch the design setup by pressing the ⁴ button.
- 3. Click on **New Design**.
- Set up the design directory to: C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram.
- 5. Set up the configuration to **AT94K**, the design name to **testram** and the tool flow to **Exemplar**, see Figure 1.
- 6. Click on the **IP Core Generator** button.
- 7. Select **Memory** from the bottom tab and **RAM-Dual Port** from the right hand tab.
- 8. Type 5 for Address Width and 4 for Width. (Address Width is 5 since $2^{5} = 32$)
- 9. Select **Asynchronous** for **RAM Type**, and type the macro name **dramasync**. Steps 6, 7, and 8 are shown in Figure 2.

Figure 1. New Design Window

New Design		×
Design Name:	Design Directory:	ок
testram	c:\SystemDesigner\examples\at94k\ATSTk	Cancel
	examples	
	ATSTK94 Designs	Help
Files of Type:	Drives:	
EDIF Netlist (*.edf)	c:\:	
Configuration:		
АТ94К	•	
Tools Flow:	Tools Flow Description:	
Exemplar-MTI	Import Net : EDIF	
Everest-VHDL	Export Net : Flat VHDL	
Orcad	Export Delay : Flat/Hier. SDF	

If there is no user library, click on the Browse button to add a new library.
 By default, IDS creates user94k.lib, if this file was not created, refer to the Create a

New Library section on page 9 for more details.

11. Now click on the Generate button.

After finishing generating this RAM block, IDS brings up a dialog box, see Figure 3.

12. Click on **OK** to dismiss the dialog box, and click on **CANCEL** to dismiss IP Core Generator.

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Figure 2. A	T94K IP Co	re Generator	Window
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	erators		_ 🗆
Address Width	5	FIFO	
Midth	4	RAM-Dual Port	
External decoding	•	RAM-Single Port	2
Clustered	O Distributed	ROM	
RAM Type			
C Synchronous	Asynchronous		
Invert Clock			
	Memory Register		
	Memory Register	Options	
DSP 10 Log Macro Name	Memory Register	Options Hard Macro	
DSP 10 Log Macro Name Pin Map File Name	Memory Register	Options Mard Macro Generate S	chematic
■ DSP 1/0 Log Macro Name Pin Map File Name Jser Library	Memory Register dramasync	Options Hard Macro Generate S Browse	chematic Batch Size

Follow the steps below to instantiate this RAM component in the **testram.vhd** file. The **dramasync.vht** file is located under:

C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\user94k\dramasync.

1. Copy the contents of **dramasync.vht** and paste them onto **testram.vhd** as shown below. Paste the words in *Italic*, and type manually the words in **bold**.





```
READN : IN std_logic
);
END testram ;
ARCHITECTURE behv OF testram IS
Component dramasync
port (
        DOUT : out std_logic_vector(3 downto 0);
        AIN : in std_logic_vector(4 downto 0);
        AOUT : in std_logic_vector(4 downto 0);
        DIN : in std_logic_vector(3 downto 0);
        OEN : in std_logic;
        WEN : in std_logic;
);
end component;
```

```
BEGIN
```

```
U1 : dramasync
```

```
PORT MAP(

DOUT => DATAOUT,

AIN => ADDRIN,

AOUT => ADDOUT,

DIN => DATAIN,

OEN => READN,

WEN => WRITEN

);
```

END behv;

Macro - drar	nasyne
Macro Performance (using -1 s	peed grade) ———
Speed :	128.7 MHz
Critical Path Delay :	7.8 ns
Power Consumption :	" mAMHz
Logic Size (x*y) :	1x1 logic cells
Logic Size (x^y) :	1x1 logic cells
Equivalent FIL Gates :	N/A

Figure 3. AT94K IP Core Generator Statistics Window

After modifying the **testram.vhd** file, the code needs to be synthesized to generate the "edf" file.

- 1. Click on the button on the IDS window, the LeonardoSpectrum window appears.
- 2. Browse to select testram.vhd file.
- 3. Change the technology to **AT94K**, then click on **Run Flow**. If an error appears, check the **testram.vhd** file again.

Figure 4 is an example of an LeonardoSpectrum window with all the correct setup.

4. After generating the **testram.edf** file, close LeonardoSpectrum and return to the IDS main window.





Figure 4. Exemplar Logic - LeonardoSpectrum Window

🈸 Exempler Logic - LeonardoSp	ectrum Level 1 Atmel - [Inform	ation - Read Only]	
15 Eile Edit View Icols Options	: <u>W</u> indow Flows <u>H</u> elp		_ 3 ×
👪 🛅 🏦 🖼 🖼 🔟	🖸 🗗 🔯 🗇 🖉 🖻	🖬 🖉 🕺 K M 🖻 🖻 🖉 👘	
Quick Techn Input Const Run the entire synthesis flow from P Res(s), technology and desired freq testian vhd	t Optimi Dutput Back is one condensed page. Specily uency, then press Run Flow.	optimize -target at94k -effort Start optimization for design Start timing optimization for No critical paths to optimize at Cell: testram View: behv Li	guick -chip -area -hier
Open files Output File: C:Vechan/Vechan.edf	بر ۲ آ	Mumber of ports : Sumber of nets : Sumber of instances : Number of references to this vie	20 40 21 ¥ 1 0
Technologies:	Device:	Total accumulated area :	
Co. Almel		Black Box dramasync :	1
AT40K	-	Mamber of ibuf :	16
ATEK02	Speed Brade:	Bunker of obuf :	4
ATEKD4 ATEK		Design summary in file 'C:/tes Start LUT decomposition for de Writing file C:/testram/testra CPU time taken for this run wa Run Successfully Ended On Tue 0	tram/testram.sum' sign .work.testram.bebw m.edf s 1.37 sec Now 28 16:32:16 Pacific
Hierarchy	E Frank (Comparison Film	 Info: Finished Synthesis run 	
	Extended Uptimization Effc		
Run Flow	Help		기
Active Perview		Transcript Filtered Transcript	
Ready		Working Directory: D. Work	Line 169 Col 1

The step below imports the testram.edf file into IDS.

- 1. Click on the **Open** button and select **Design**.
- 2. Change the **Files of Type** box to ***.edf**; IDS automatically selects the **testram.edf** file, see Figure 5.
- 3. Click on **OK**. The design browser appears.
- 4. Click on the Map button. The mapping browser appears.
- 5. Click on the **Parts** button to select the part . This example uses **AT94K40-25DQC**.
- 6. Click on the **Compile** button.
- 7. Click on the button. IDS will generate back-annotated vhdl and test bench files for simulation purposes.

The vhdl files are located under:

C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\figba

Figure 5. Open a Design Window

Design Directory:		OK
c:'testram		Cancel
Design Name:	Files of Type:	
testram	EDIF Netlist (*.edf)	Hein
Tools Flow:	Configuration:	
Exemplar-MTI	Ат94К	New Design
Existing Design File:		<u> </u>

Check the Design	To check the design with simulation, copy:
with Simulation	C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\testram_test_bench.vhd to
	C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\figba\testram_test_bench.vhd.

- 1. Open the ModelSim window.
- 2. Click on File > Change directory.
- 3. Browse to the C:\System Designer\examples\at94k\ATSTK94 Designs\Ram\figba\ directory and click on OPEN.
- To setup the ModelSim library, on the window, type the following commands:
 vlib work
 - vmap work ./work
- 5. Click on **Design > Compile**
- 6. Select dramasync.vhd and click on Compile.
- 7. Select testram.vhd and click on Compile.
- 8. Select testram_test_bench.vhd and click on Compile.
- 9. Click on **Done** to dismiss the dialog.
- 10. Go to **Design > Load New Design**.
- 11. Select **post_test_bench** and click on **Load**, see Figure 6.
- 12. Go back to the ModelSim window and type the following command:
 - Add wave –r /*
 - Run –all
- 13. Let it run for 50 microseconds
- 14. Go to the wave window and click the 🕅 button.





Figure 6. Load Design Window

Load Design		
Design VHDL Verilog	3 SDF	
Simulator Resolution:	default 🔟	
Library: work	±	Browse
Simulate:		Add
Design Unit	Description	
dramasync	Entity	
 post_test_bench testram 	Entity	
		1
Load	Exit Save Settings Ca	ncel

15. A waveform similar to the one shown in Figure 7 appears.

16. Check the results.

Note: This design has loaded values 0000 to 1111 to memory locations 00000 to 01111 respectively. Later it will read back from those memory locations. The signal READN is asserted for 100 ns and de-asserted for 100 ns, some undefined states in between the DATAOUT will be visible.

Figure 7. Wave Window

🔫 wave - default		
<u>File Edit Cursor Zoom Format Windo</u>	W	
😅 🖬 🎒 🕴 🖧 🗎 🛍 🛍 🗎 📐 🔏 📑	+ →	
 /post_test_bench/sig_dataout_0 /post_test_bench/sig_dataout_1 /post_test_bench/sig_dataout_2 /post_test_bench/sig_dataout_3 	00000××××	
		500 us 1 ms
	Ups	
	• •	•
0 ps to 1332886128 ps		1.

Create a New Library

Follow the steps below to set up a new user library:

- 1. Click on Library on IDS main window.
- 2. Select Library Setup, see Figure 8.
- 3. Click on Add Before.
- 4. Select the directory, type the library name and then click on **OK**, see Figure 9 on page 10.
- 5. Click on **OK** to dismiss the Library Setup.





Figure 8. Library Setup Window

Library Coaronn an	_	OK
o Vootvoo	Add Before	Cancel
civestram	Add After	
		Help
	Remove	
Library Names	1	
 user94k (c:\testram\user94k lib)	Add	
	Create	

Figure 9. Add Library Window

orary Name:	Directories:	ок
user94k.lib	c:\testram	Add All
iser94k.lib	C:\	Cancel
	figba user94k	Help
t Files of Type:	Drives:	

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Atmel Headquarters

Corporate Headquarters 2325 Orchard Parkway San Jose, CA 95131 TEL (408) 441-0311 FAX (408) 487-2600

Europe

Atmel SarL Route des Arsenaux 41 Casa Postale 80 CH-1705 Fribourg Switzerland TEL (41) 26-426-5555 FAX (41) 26-426-5500

Asia

Atmel Asia, Ltd. Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimhatsui East Kowloon Hong Kong TEL (852) 2721-9778 FAX (852) 2722-1369

Japan

Atmel Japan K.K. 9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL (81) 3-3523-3551 FAX (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs 1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL (719) 576-3300 FAX (719) 540-1759

Atmel Grenoble

Avenue de Rochepleine BP 123 38521 Saint-Egreve Cedex, France TEL (33) 4-7658-3000 FAX (33) 4-7658-3480

Atmel Heilbronn

Theresienstrasse 2 POB 3535 D-74025 Heilbronn, Germany TEL (49) 71 31 67 25 94 FAX (49) 71 31 67 24 23

Atmel Nantes

La Chantrerie BP 70602 44306 Nantes Cedex 3, France TEL (33) 0 2 40 18 18 18 FAX (33) 0 2 40 18 19 60

Atmel Rousset

Zone Industrielle 13106 Rousset Cedex, France TEL (33) 4-4253-6000 FAX (33) 4-4253-6001

Atmel Smart Card ICs

Scottish Enterprise Technology Park East Kilbride, Scotland G75 0QR TEL (44) 1355-357-000 FAX (44) 1355-242-743

Atmel Programmable SLI Hotline (408) 436-4119

Atmel Programmable SLI e-mail fpga@atmel.com – fpslic@atmel.com

FAQ Available on web site

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Fax-on-Demand North America: 1-(800) 292-8635 International: 1-(408) 441-0732 *e-mail* literature@atmel.com

Web Site http://www.atmel.com

BBS 1-(408) 436-4309