Accessing 16-bit I/O Registers

Features

- **Routines for Accessing 16-bit I/O Registers**
- **Macros Included for the FPSLIC™ AVR® Core and IAR C Compiler**

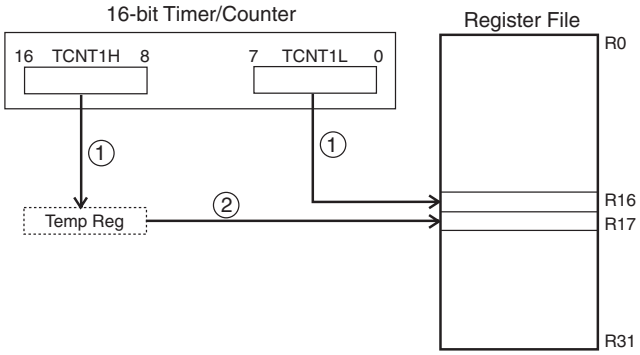
Description

All FPSLIC devices include a 16-bit timer. These I/O modules have 16-bit registers that can be accessed from the FPSLIC AVR core using the *in* and *out* instructions. Because the FPSLIC microcontroller has an 8-bit I/O bus, access to the I/O register must be performed in two instruction cycles. An interrupt can occur between the instructions. If the interrupt function accesses the same resources (16-bit timer), the 16-bit I/O register access must be made an atomic operation, i.e., an operation that cannot be interrupted.

I/O modules with 16-bit registers include a temporary register for the high byte (bits 15 to 8). Note that the 16-bit timer (timer 1) has only one temporary register that is shared between all its 16-bit register pairs. A 16-bit I/O read is normally done like this:

```
Cycle 1:    in  r16, TCNT1L          ;Reading low byte into r16,this
                                      triggers the high byte to be latched
                                      in the temporary shadow register.
Cycle 2:    in  r17, TCNT1H          ;Reading high byte from the temporary
                                      register.
```

Figure 1. 16-bit I/O Register Read



Note: Circled numbers indicate cycle number.

If an interrupt occurs between the two instructions for any of the operations and the interrupt handler accesses any of the timer 1's low bytes, the temporary register might change its value. Returning from the interrupt, the FPSLIC AVR core now reads the corrupted value into register R17.

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10K - 40K Gates of AT40K FPGA with 8-bit AVR® Microcontroller and 36K Bytes of SRAM

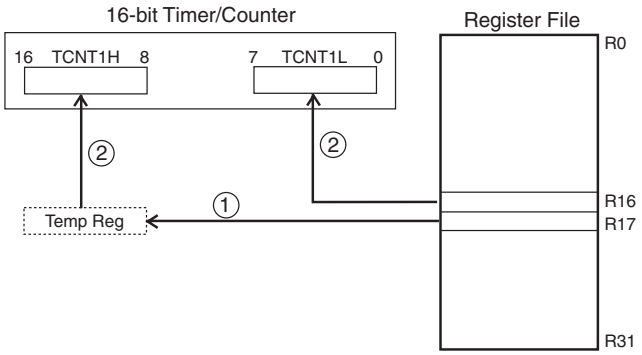
Application Note

Rev. 1980A–11/00

A 16-bit I/O write is done as follows:

```
                                    ; r17 contains the high byte while r16
                                    ; contains the low byte that is to be
                                    ; written.
Cycle 1:    out   TCNT1H, r17       ; Writing the high byte to the
                                    ; temporary register.
Cycle 2:    out   TCNT1L, r16       ; Writing both the low byte and the
                                    ; temporary register into the I/O register.
```

Figure 2. 16-bit I/O Register Write



Note: Circled numbers indicate cycle number.

Note that the read and the write operations differ in the order the high and low I/O register is accessed. If the order is reversed, the high value will be incorrectly read or written.

Solution

To avoid the situations described above, the following macros for the AVR assembler and the IAR C compiler can be used.

AVR Assembler Macros

```
.macro outw
  cli
  out     @2, @0
  out     @2-1, @1
  sei
.endmacro

.macro    inw
  cli
  in      @2, @0-1
  in      @1, @0
  sei
.endmacro
```

Usage

```
.include "AT94Kdef.inc"
inw       r17, r16, TCNT1H                  ; Reads the counter value (high, low, adr)
outw      TCNT1H, r17, r16                  ; Writes the counter value (adr, high, low )
```

IAR C Macros

```
#include <ina90.h>

#define outw( ADDRESS, VAL )\
{\
    _CLI();
    ADDRESS = VAL;\
    _SEI();\
}

#define inw( ADDRESS, VAL )\
{\
    _CLI();
    VAL = ADDRESS;\
    _SEI();\
}
```

Usage

```
#include <ioAT94K.h>

    inw( TCNT1, i )                         ;/* Reads the counter value */
    outw( TCNT1, i )                        ;/* Writes the counter value */
```

Notes

Note: 1. The outw and the inw macros use four instruction cycles, which is the same amount of cycles the ret instruction uses. In doing so, the macros will not increase the worst case interrupt response time.

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1980A–11/00/xM