Integrated Development System
Macro Library 2

June 2002

How Volume 2 is Organized

The first section of Volume 2 is actually a continuation of Volume 1. This section lists the input/output macros.

The second section includes the physical layout drawings for all of the macros, both "Functions" and "Input/Output." Some macros may have more than one physical layout description or "shape." However, this version of the databook shows just one shape for each macro. Whenever a macro has more than one shape, its default shape (Shape 1) is shown. If necessary, future versions of the databook will include all possible shapes for each macro.

Input/Output Macro Naming Conventions

Input and output macros use the following naming conventions:

I	=	Input
O	=	Output
B	=	Bidirectional
TTL	=	TTL on input
CMS	=	CMOS on input
P	=	Pull-up on pad
D	=	Full drive
S	=	Standard slew rate
F	=	Fast slew rate
OC	=	Open collector
EN	=	Tri-state enable (z)

For example, BTTLDF is a fast, bidirectional TTL input with full drive output.

Truth Table Conventions

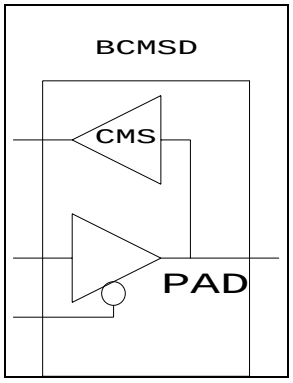
The following conventions are used in the Truth Tables:
z = Tri-State
w1 = Weak logical "one"

For More Information

If you have questions about the macro library, its use and applications, contact Atmel Customer Service by calling 408-436-4119 between 9 am to 5 pm Pacific Standard Time, or faxing 408-436-4200.

BCMSD - Bidirectional I/O CMOS Drive

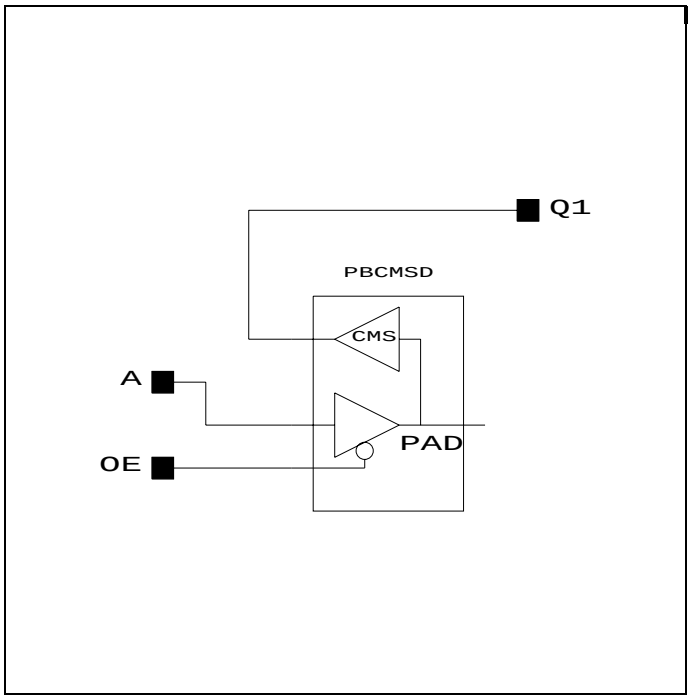
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	z	q0
0	a	a	a

Switching Speeds for -2ns Parts

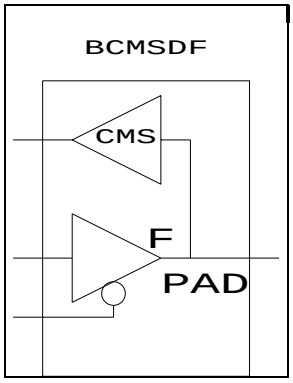
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BCMSDF - Bidirectional I/O CMOS Drive Fast

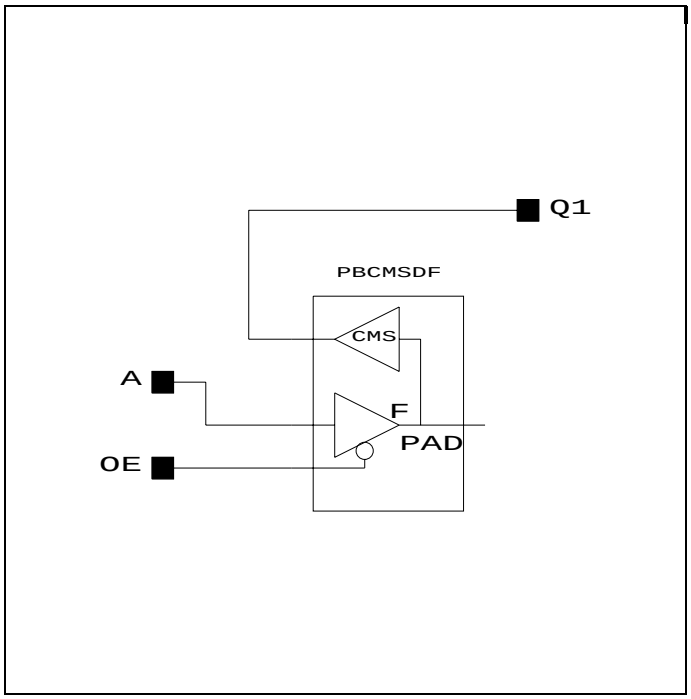
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	**OE**	**Q0**	**Q1**
x	1	z	q0
a	0	a	a

Switching Speeds for -2ns Parts

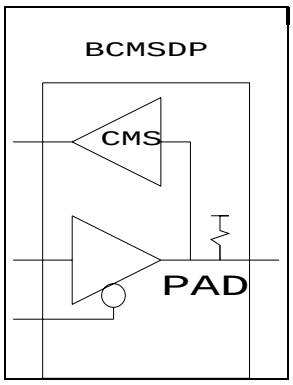
		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BCMSDP - Bidir I/O CMOS Drive with Pull-Up

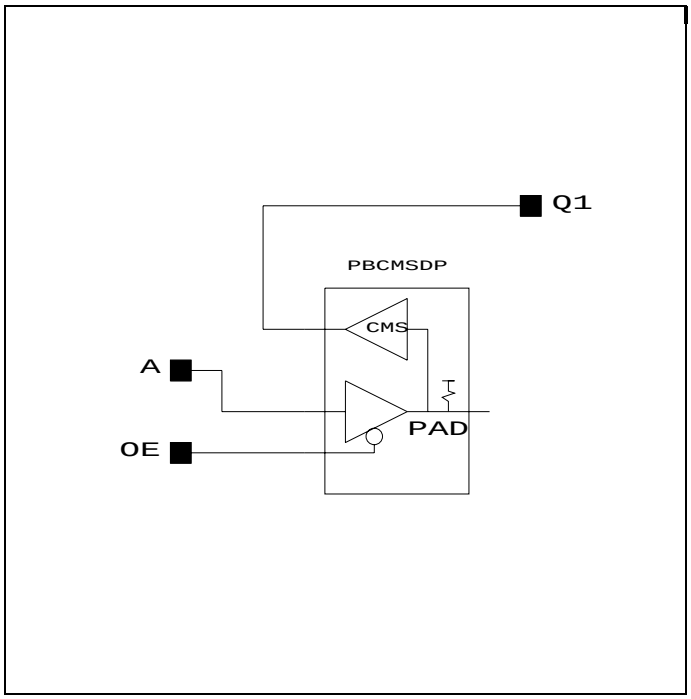
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	w1	1
0	a	a	a

Switching Speeds for -2ns Parts

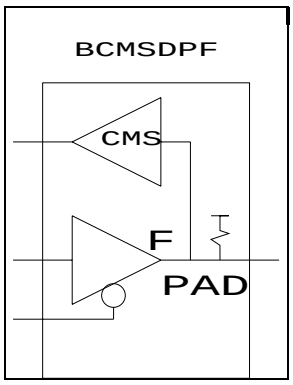
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BCMSDPF - Bidir I/O CMOS Drive with Fast Pull-Up

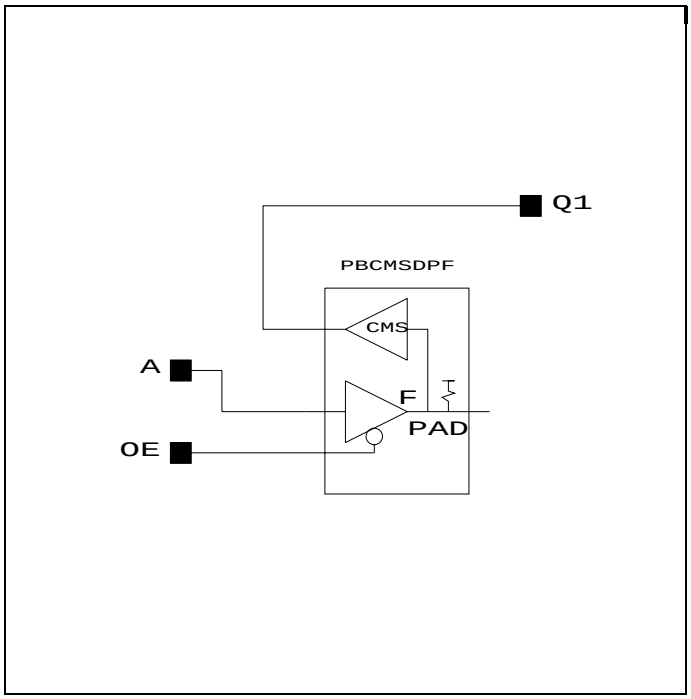
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	w1	1
0	a	a	a

Switching Speeds for -2ns Parts

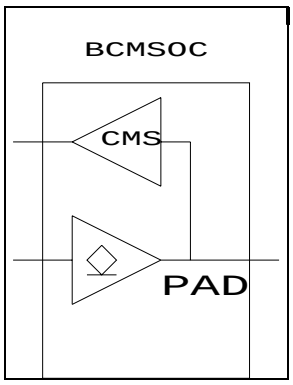
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BCMSOC - Bidirectional CMOS Open Collector

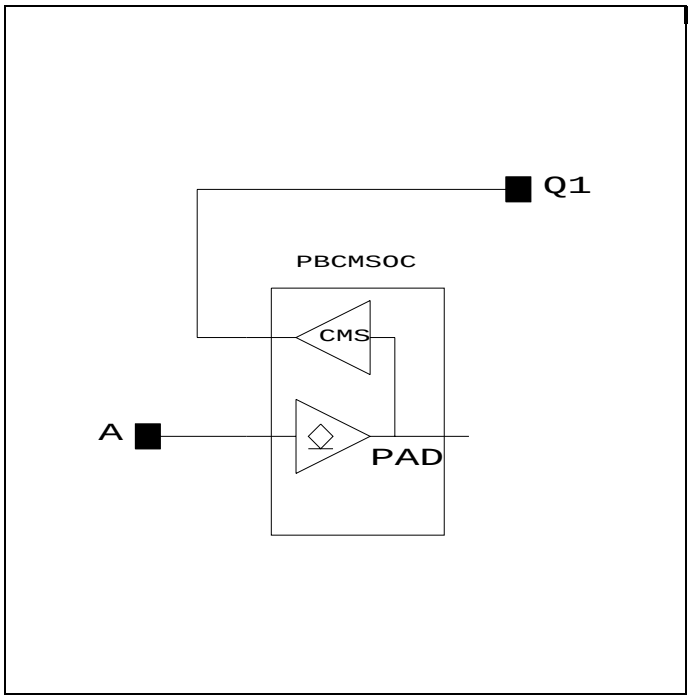
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
0	0	0
1	z	x

Switching Speeds for -2ns Parts

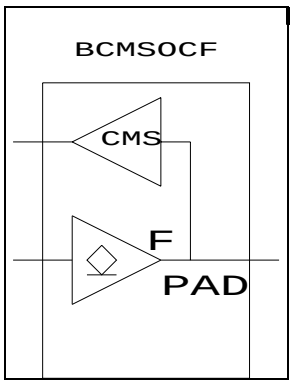
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00

BCMSOCF - Bidirectional CMOS Open Coll Fast

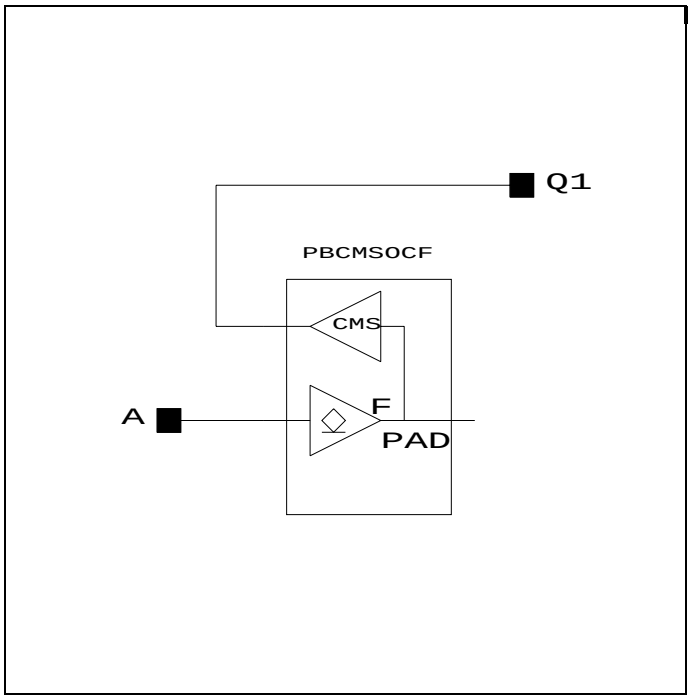
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
0	0	0
1	z	x

Switching Speeds for -2ns Parts

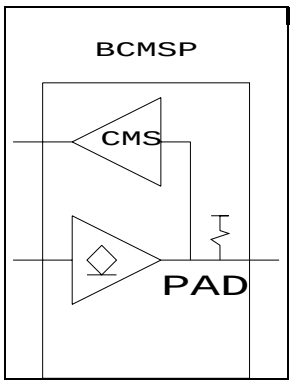
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70

BCMSP - Bidir CMOS Open Coll w/ Pull-up

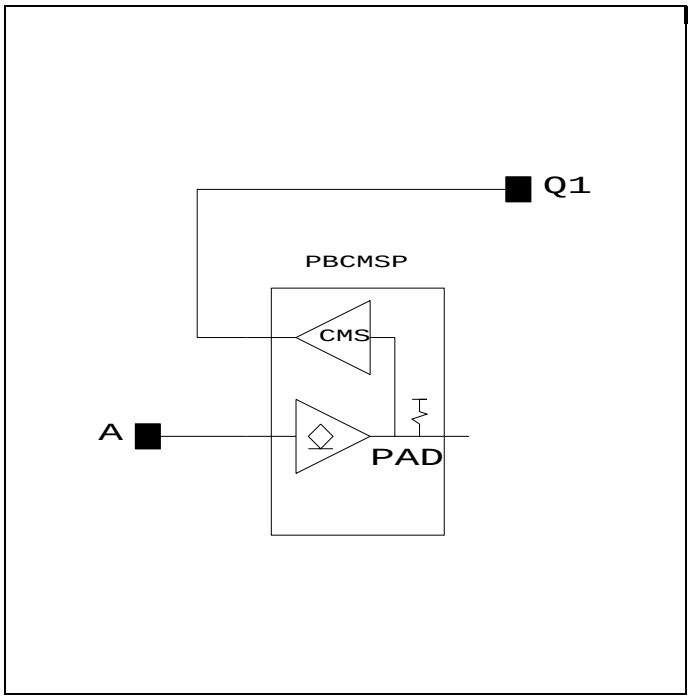
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
1	1	1
0	0	0

Switching Speeds for -2ns Parts

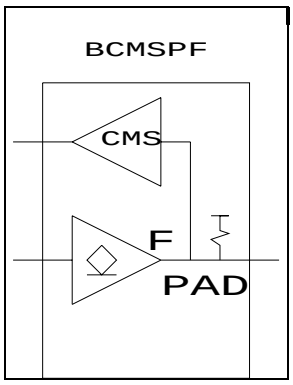
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00

BCMSPF - Bidir CMOS Open Coll Fast Pull-up

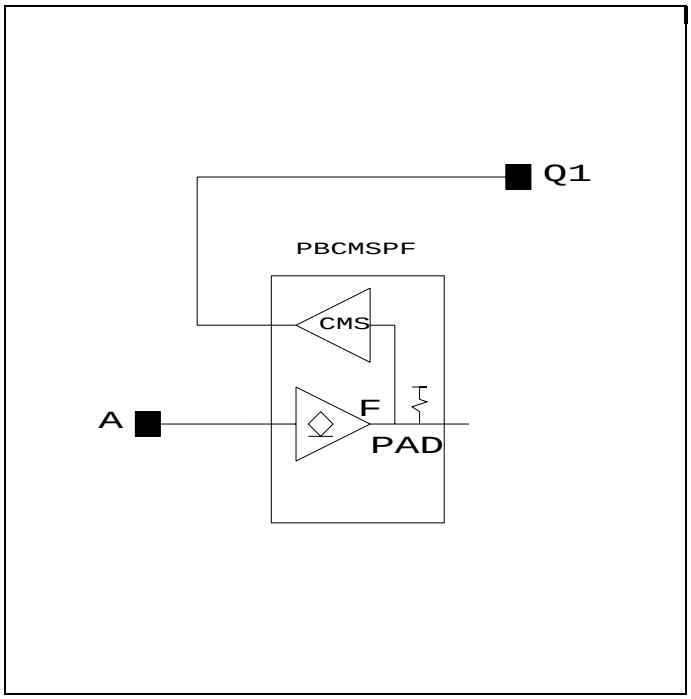
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
1	1	1
0	0	0

Switching Speeds for -2ns Parts

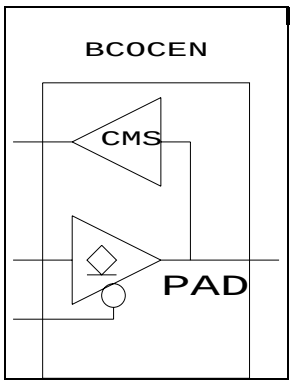
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70

BCOCEN - Bidir CMOS Open Coll w/ Enable

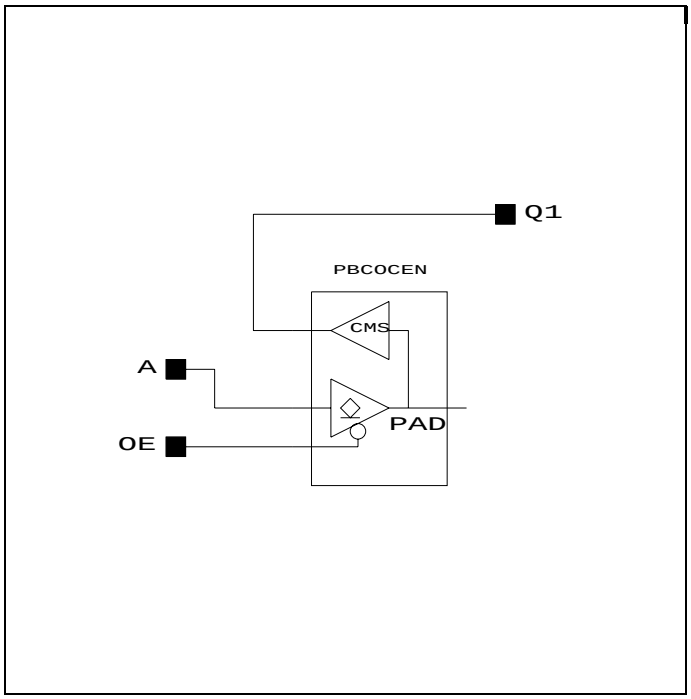
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	z	q0
0	0	0	q0
1	0	z	q0

Switching Speeds for -2ns Parts

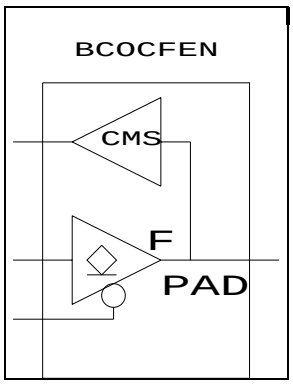
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BCOCFEN - Bidir CMOS Open Coll Fast Enable

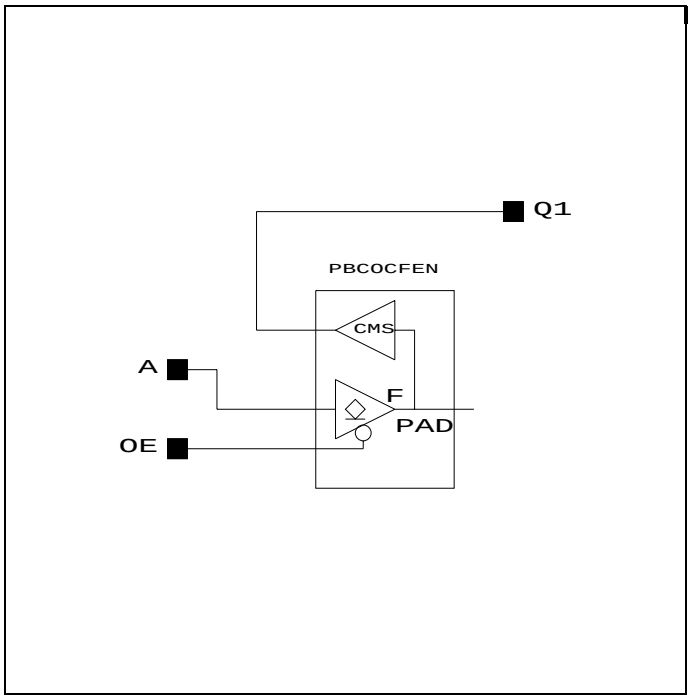
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	z	q0
0	0	0	q0
1	0	z	q0

Switching Speeds for -2ns Parts

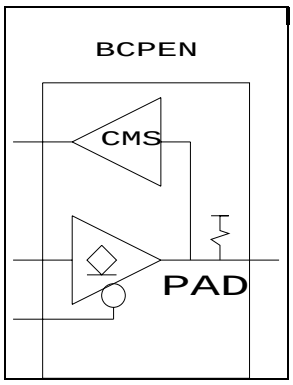
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BCPEN - Bidir CMOS Open Coll Pull-up Enable

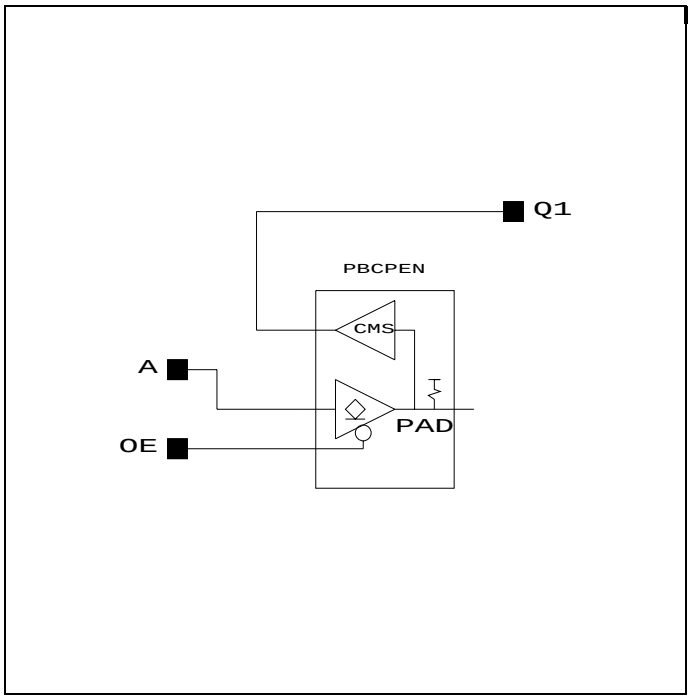
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	w1	q0
0	0	0	q0
1	0	1	q0

Switching Speeds for -2ns Parts

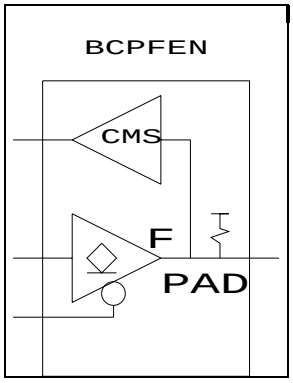
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BCPFEN - Bidir CMOS Op Coll Fst Pull-up Enable

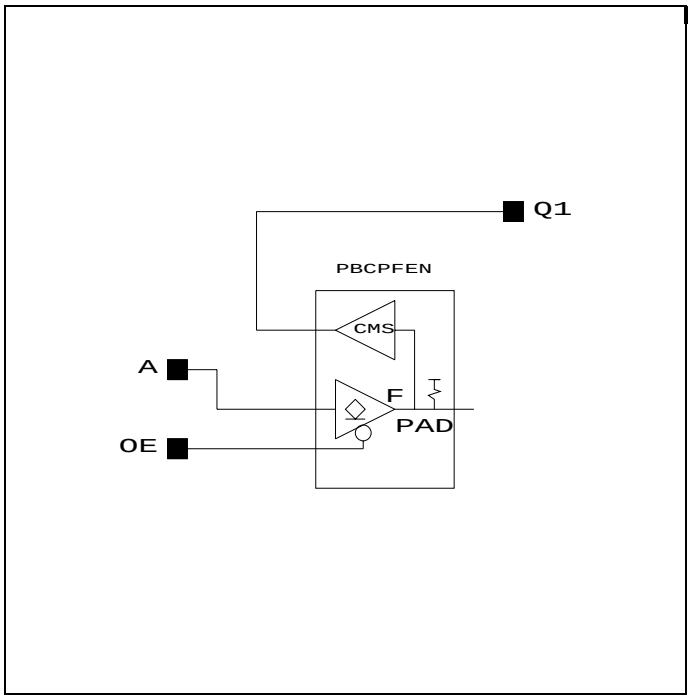
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	w1	1
0	0	0	q0
1	0	1	q0

Switching Speeds for -2ns Parts

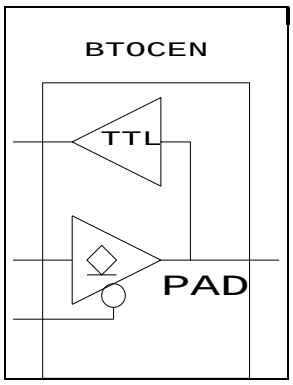
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.60	2.10	2.40	1.60	1.80	1.90
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	2.30	2.50	2.80	1.80	2.00	2.20
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BTOCEN - Bidir TTL Open Coll w/ Enable

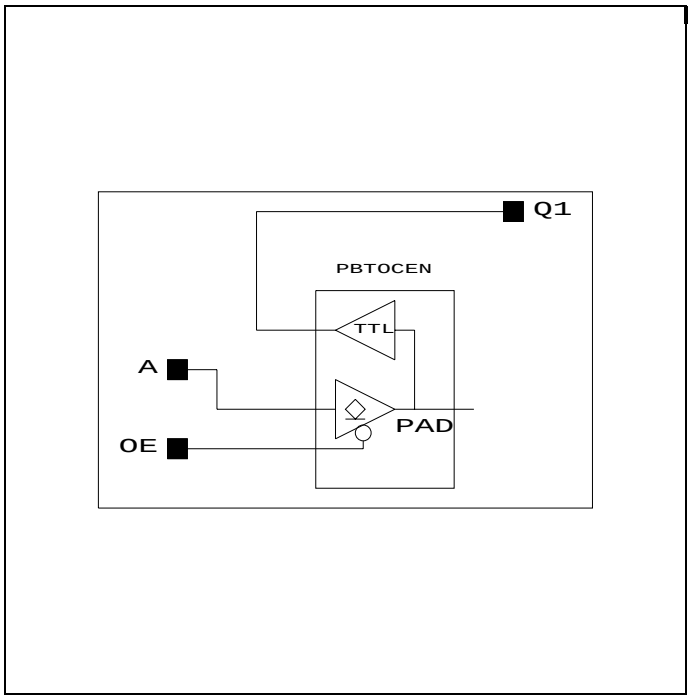
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	z	q0
0	0	0	q0
1	0	z	q0

Switching Speeds for -2ns Parts

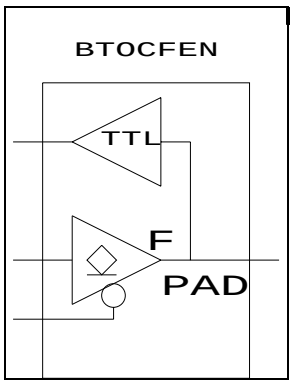
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BTOCFEN - Bidir TTL Open Coll Fast Enable

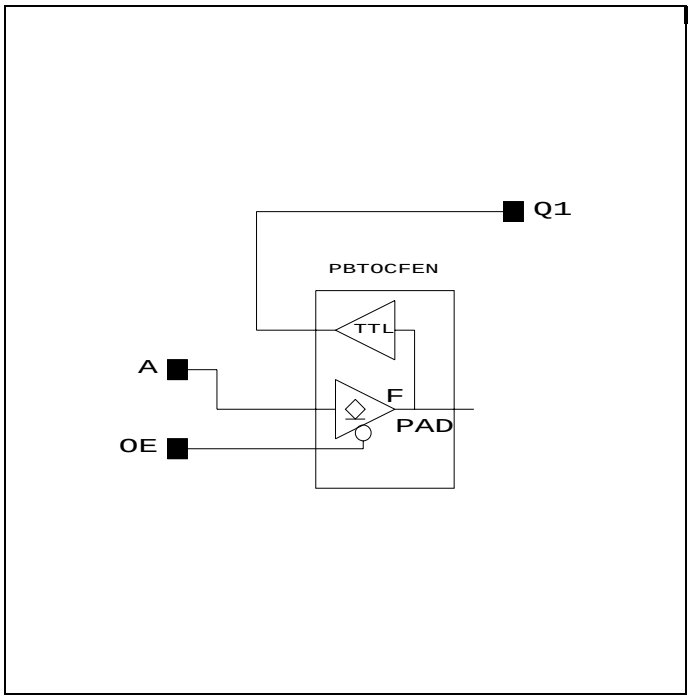
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	z	q0
0	0	0	q0
1	0	z	q0

Switching Speeds for -2ns Parts

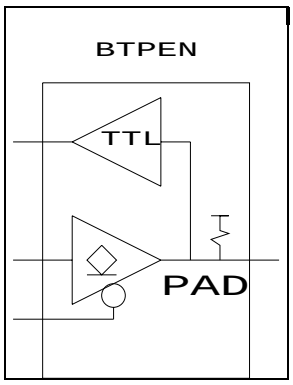
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BTPEN - Bidir TTL Open Coll Pull-up Enable

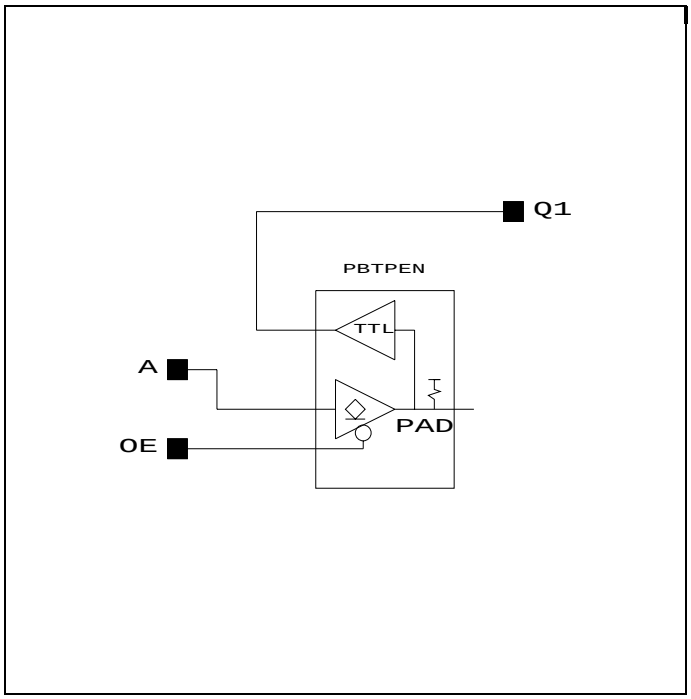
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	w1	1
0	0	0	q0
1	0	1	q0

Switching Speeds for -2ns Parts

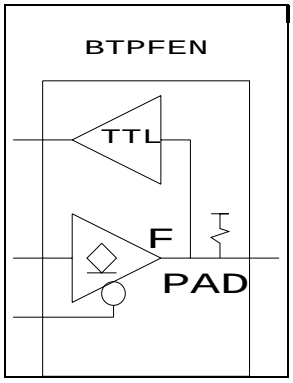
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BTPFEN - Bidir TTL Op Coll Fst Pull-up Enable

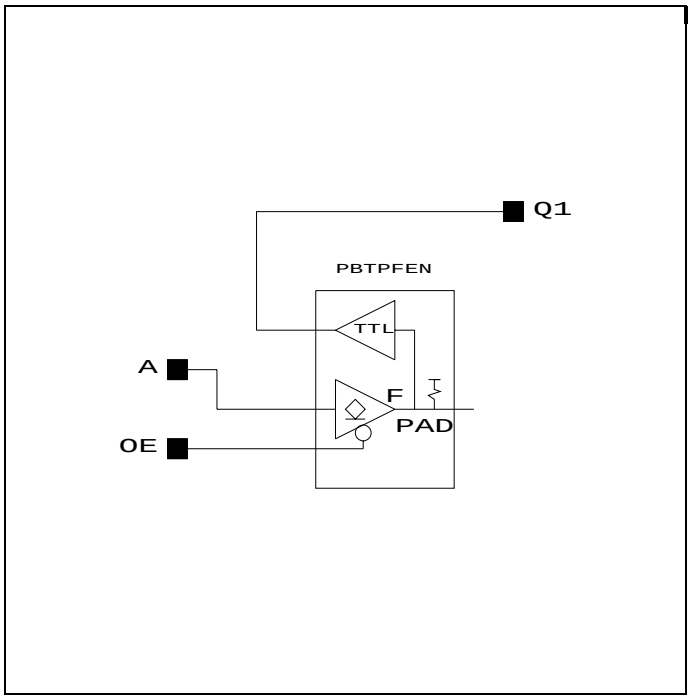
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	OE	Q0	Q1
x	1	w1	1
0	0	0	q0
1	0	1	q0

Switching Speeds for -2ns Parts

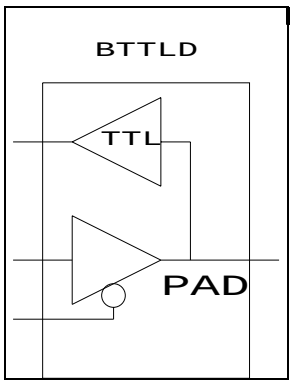
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BTTLD - Bidirectional I/O TTL Drive

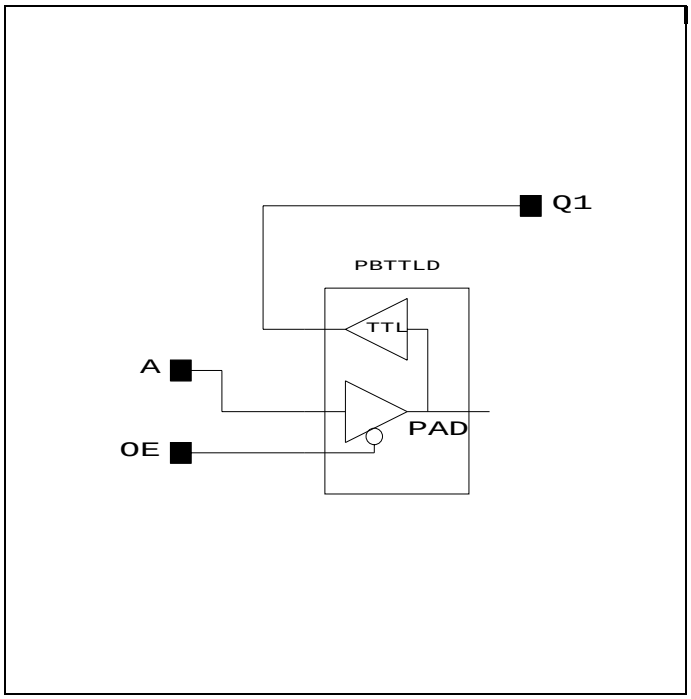
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	z	q0
0	a	a	a

Switching Speeds for -2ns Parts

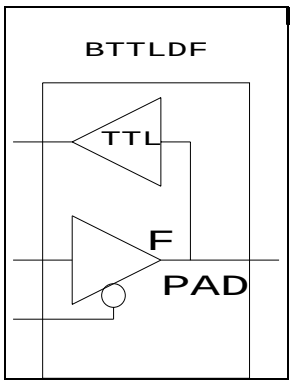
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BTTLDF - Bidirectional I/O TTL Drive Fast

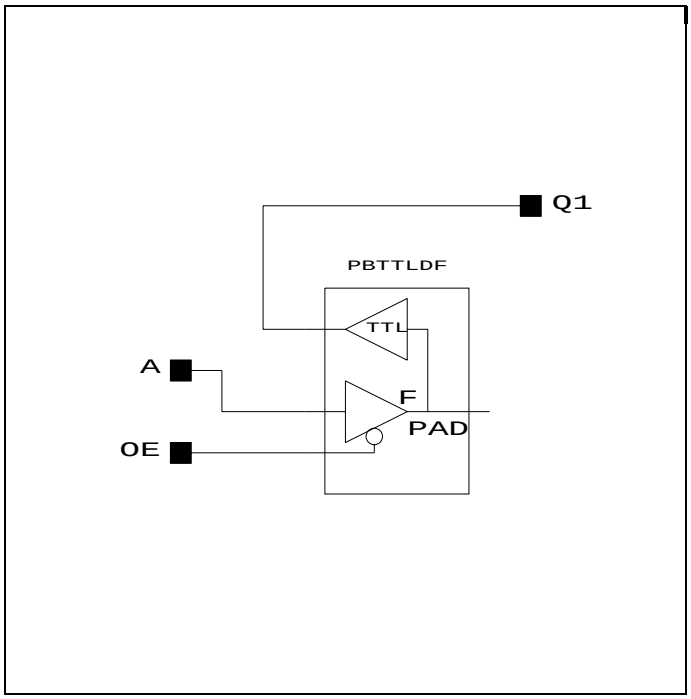
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	z	q0
0	a	a	a

Switching Speeds for -2ns Parts

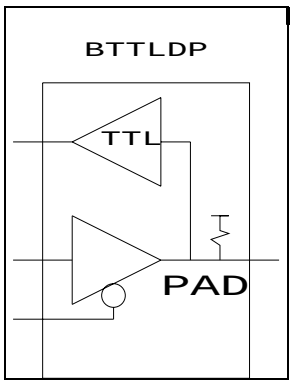
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BTTLDP - Bidir TTL Drive with Pull-up

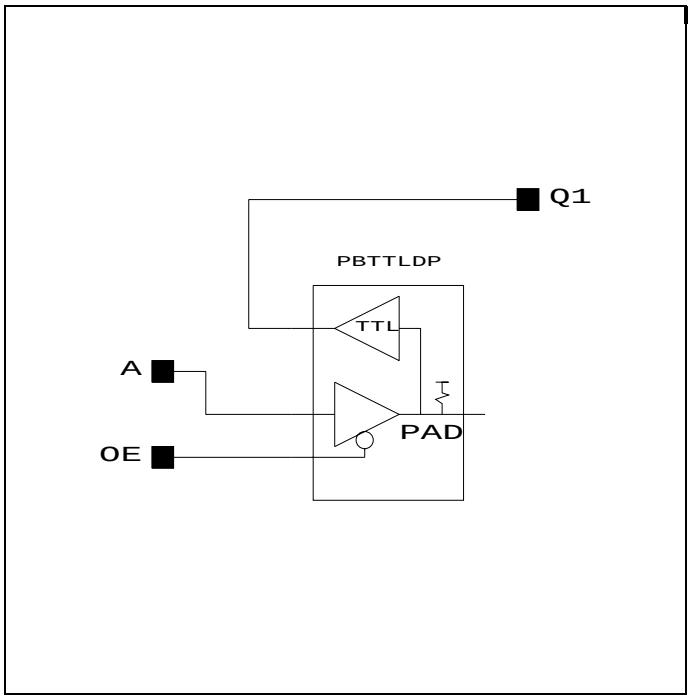
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	w1	1
0	a	a	a

Switching Speeds for -2ns Parts

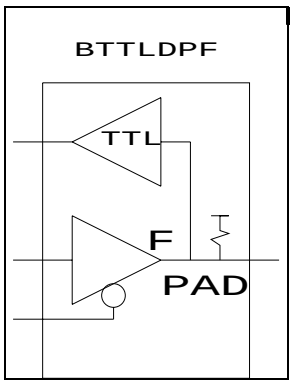
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q0	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q0	5.60	7.50	11.00	7.20	9.40	13.50

BTTLDPF - Bidir TTL Drive with Fast Pull-up

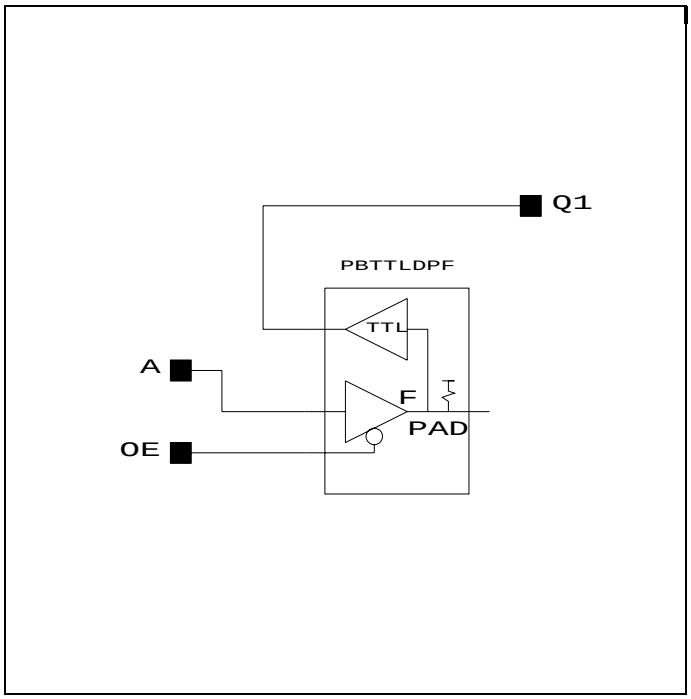
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
OE	A	Q0	Q1
1	x	w1	1
0	a	a	a

Switching Speeds for -2ns Parts

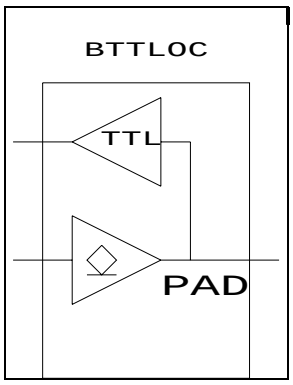
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q0	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q0	2.80	4.50	7.10	3.20	4.60	7.20

BTTLOC - Bidirectional TTL Open Collector

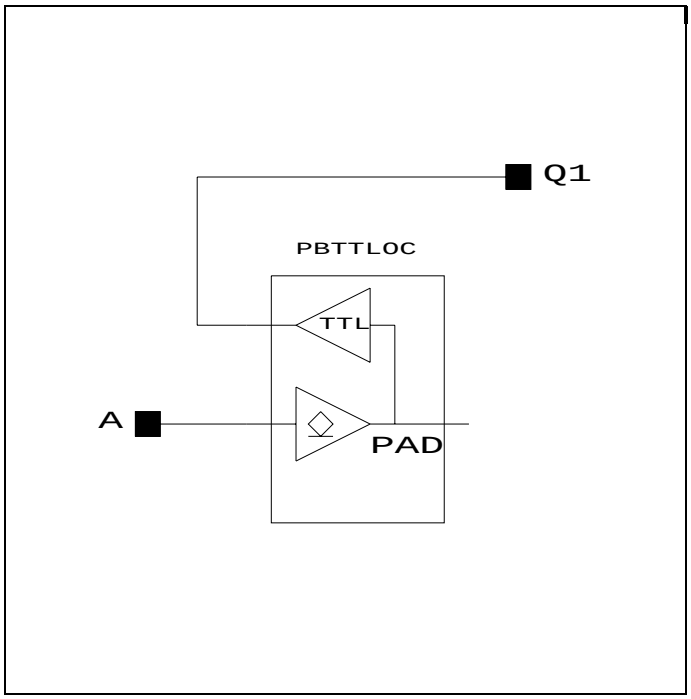
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
0	0	q0
1	z	q0

Switching Speeds for -2ns Parts

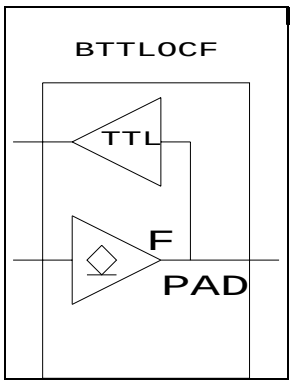
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00

BTTLOCF - Bidirectional TTL Open Coll Fast

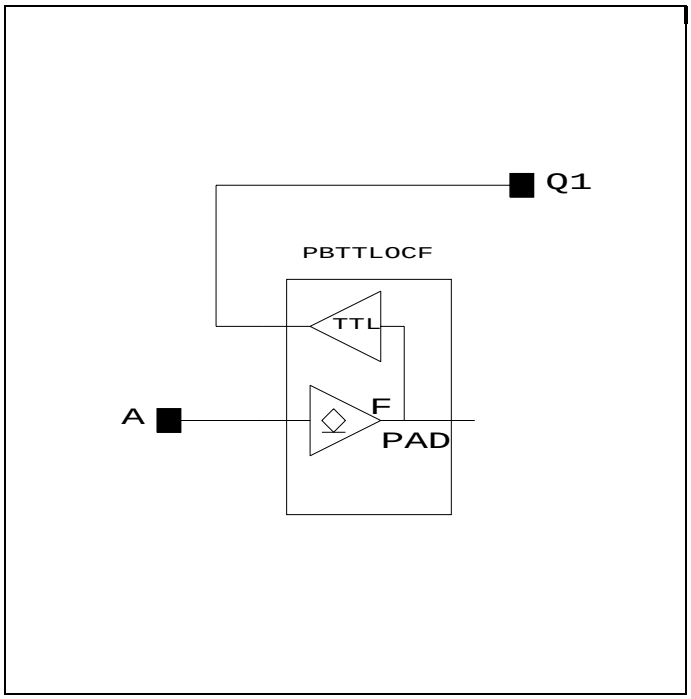
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
0	0	q0
1	z	q0

Switching Speeds for -2ns Parts

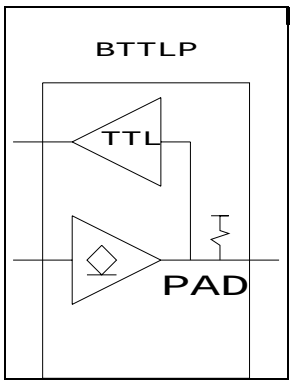
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70

BTTLP - Bidir TTL Open Collector w/ Pull-up

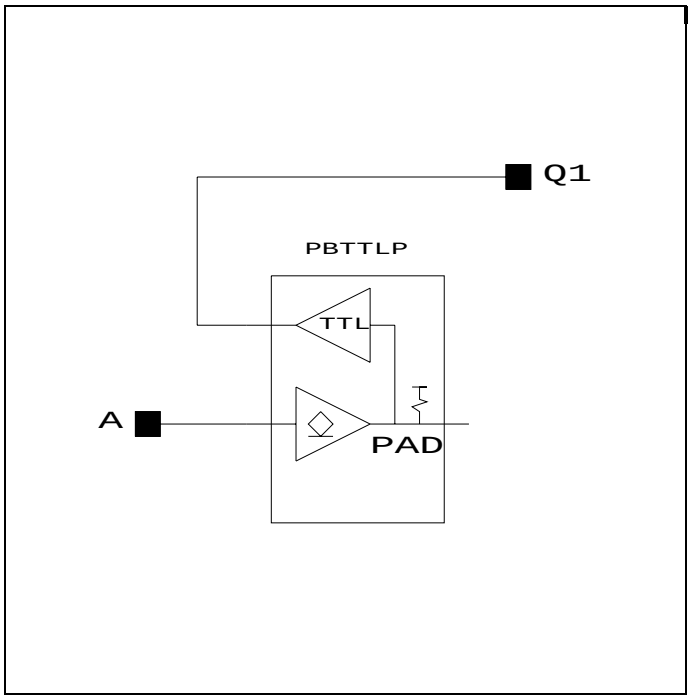
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
1	w1	1
0	0	q0

Switching Speeds for -2ns Parts

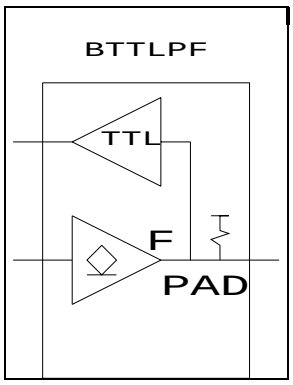
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	6.10	8.00	11.60	7.60	9.90	14.00

BTTLPF - Bidir TTL Open Collector w/ Fast Pull-up

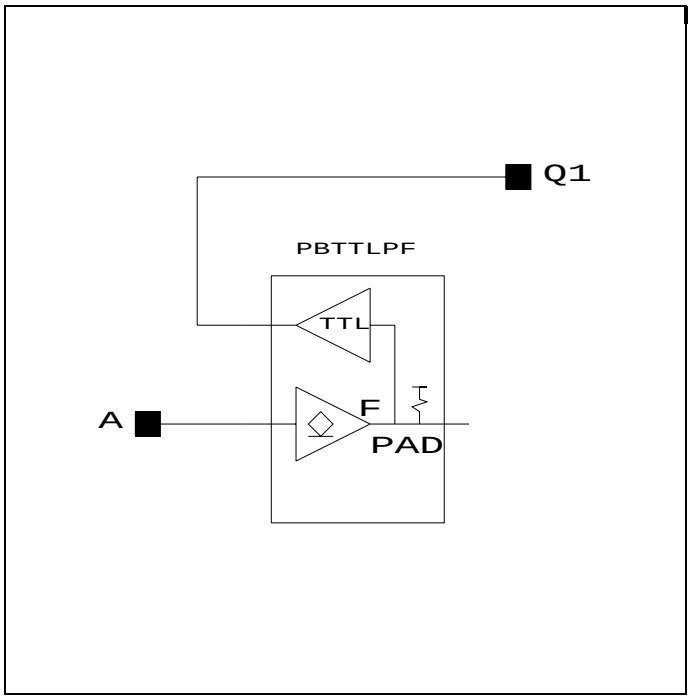
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1
1	w1	1
0	0	q0

Switching Speeds for -2ns Parts

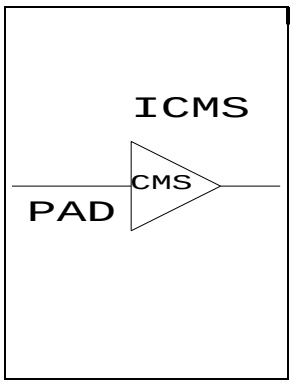
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	0.90	1.00	1.10	1.40	1.60	1.80
A → Q0	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
Q0 → Q1	1.40	1.50	1.70	1.40	1.50	1.70
A → Q0	3.30	5.00	7.60	3.60	5.10	7.70

ICMS - Input Buffer CMOS Level

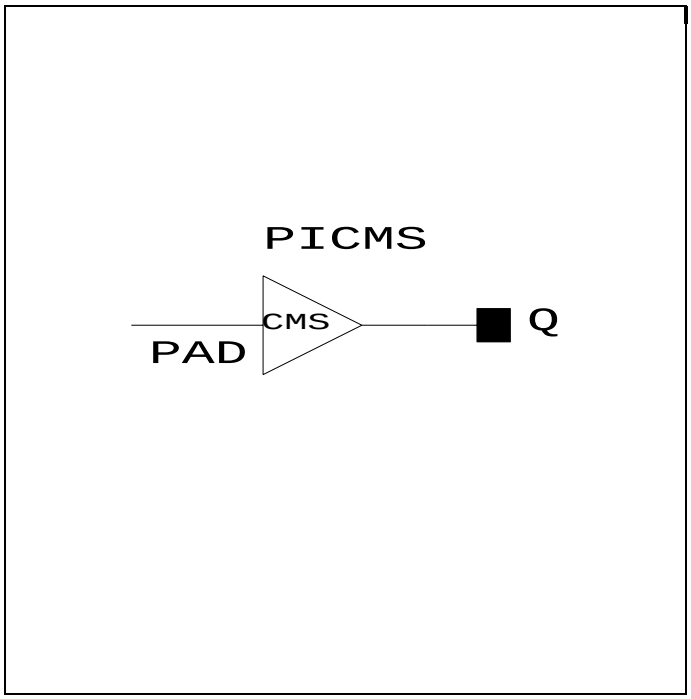
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

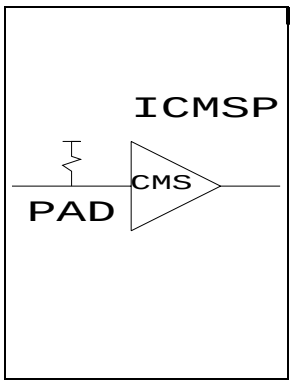
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.60	2.10	2.40	1.60	1.80	1.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.30	2.50	2.80	1.80	2.00	2.20

ICMSP - Input Buffer CMOS Level with Pull-up

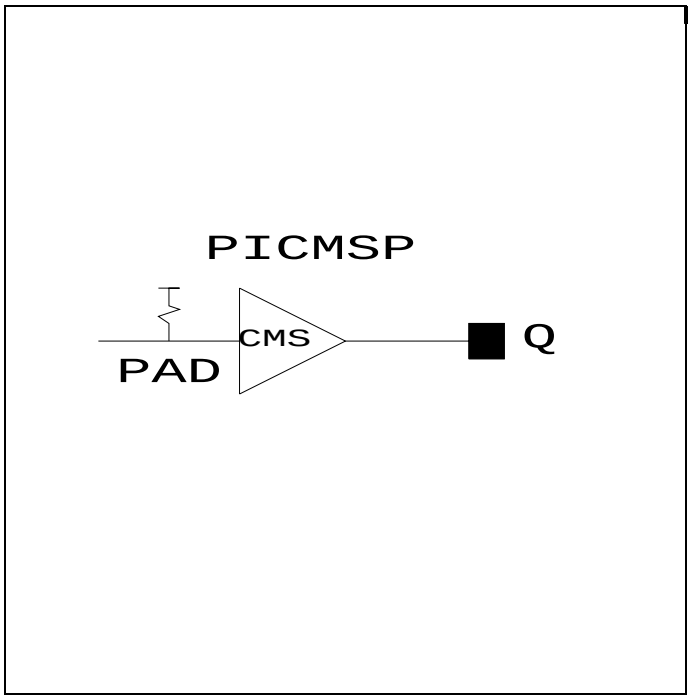
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

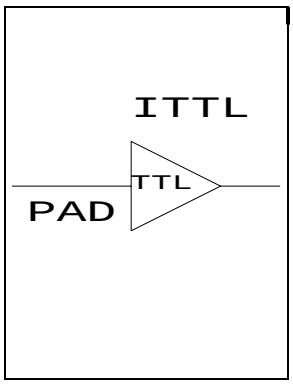
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.60	2.10	2.40	1.60	1.80	1.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.30	2.50	2.80	1.80	2.00	2.20

ITTL - Input Buffer TTL Level

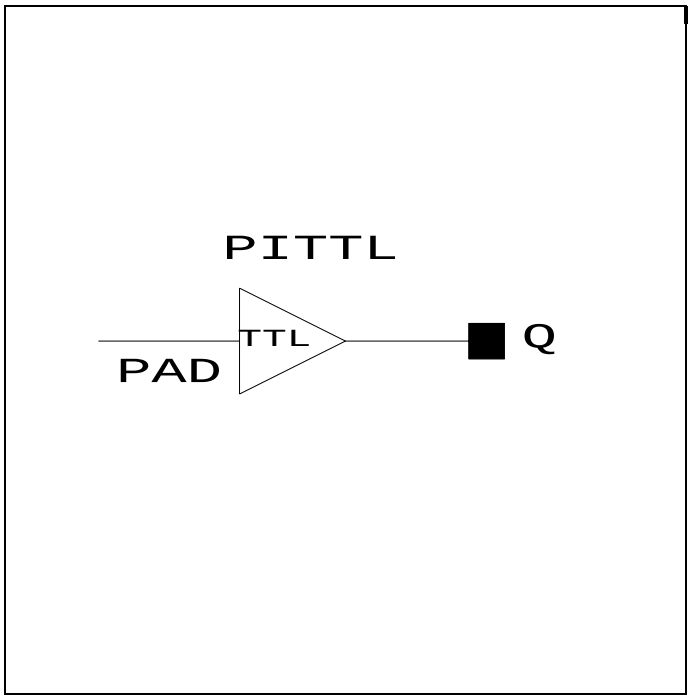
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

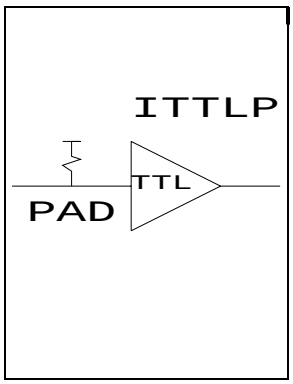
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.90	1.00	1.10	1.40	1.60	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.40	1.50	1.70	1.40	1.50	1.70

ITTLP - Input Buffer TTL Level with Pull-up

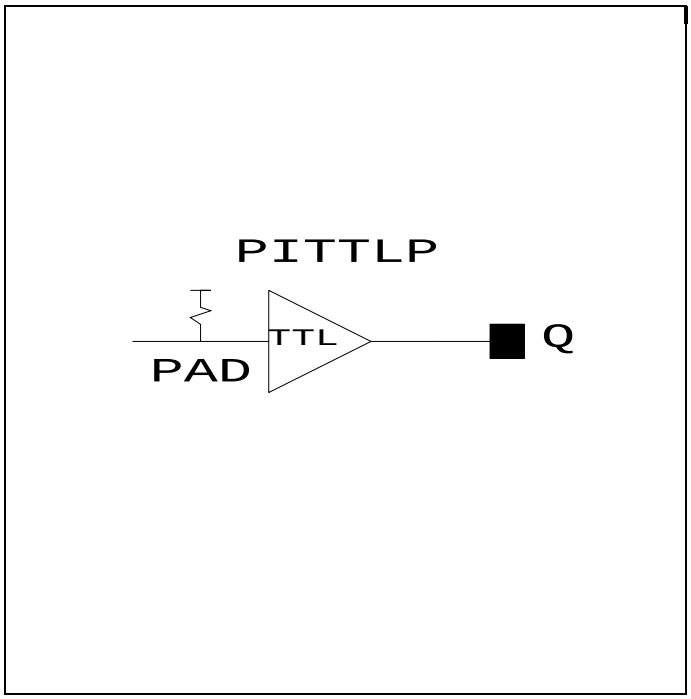
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

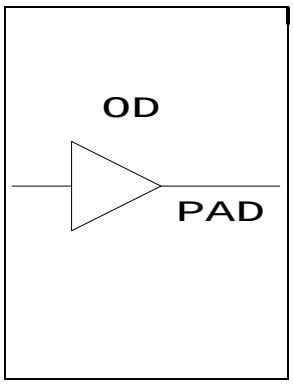
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.90	1.00	1.10	1.40	1.60	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.40	1.50	1.70	1.40	1.50	1.70

OD - Output Buffer Drive

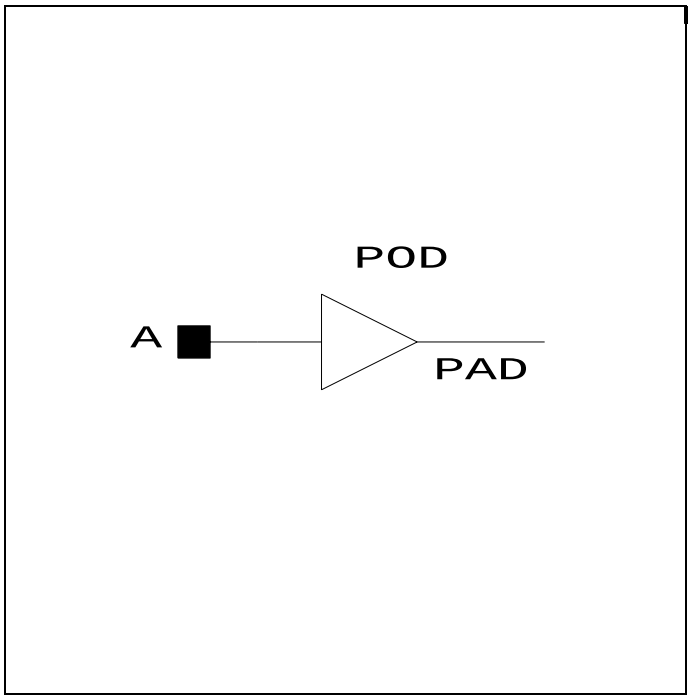
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

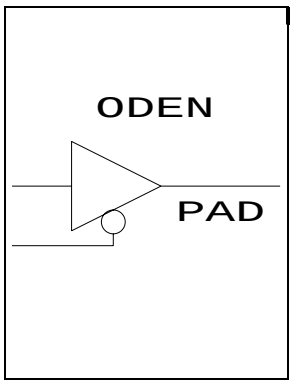
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00

ODEN - Tristate Output Drive

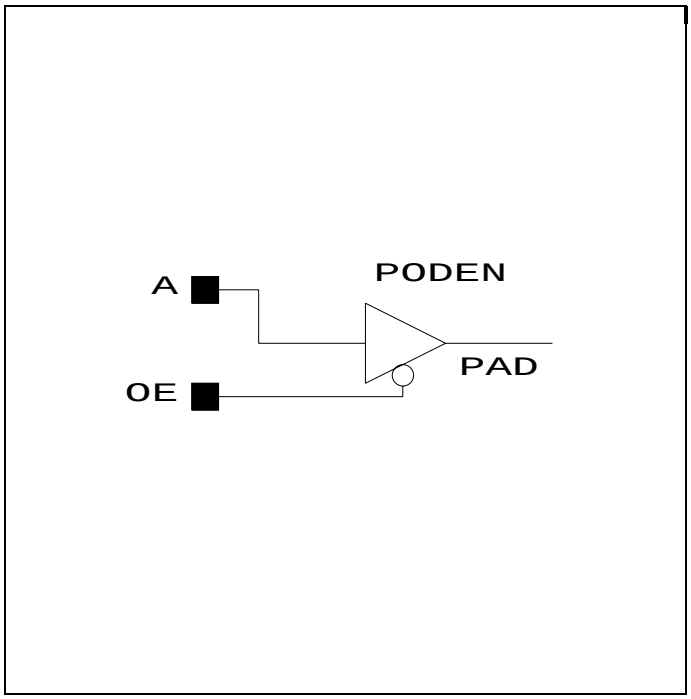
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output
OE	A	Q
1	x	z
0	a	a

Switching Speeds for -2ns Parts

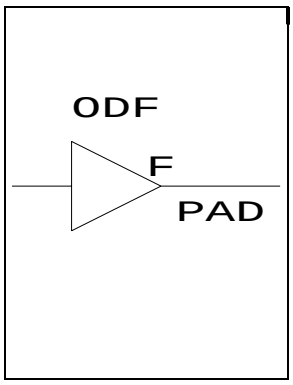
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q	5.60	7.50	11.00	7.20	9.40	13.50

ODF - Output Buffer Drive Fast

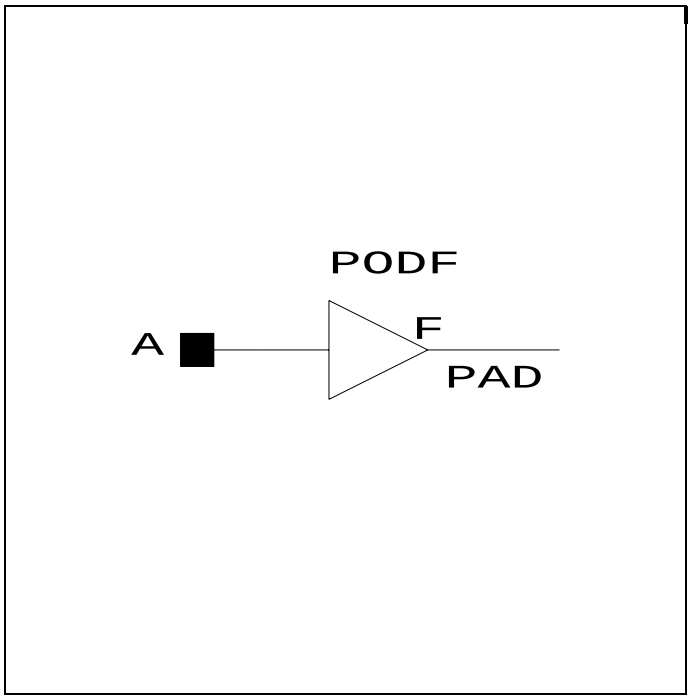
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

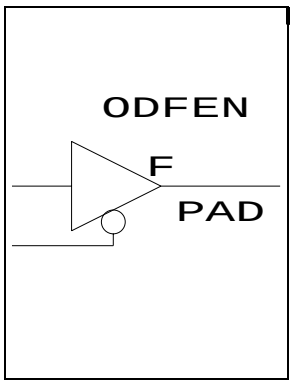
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70

ODFEN - Tristate Output Drive Fast

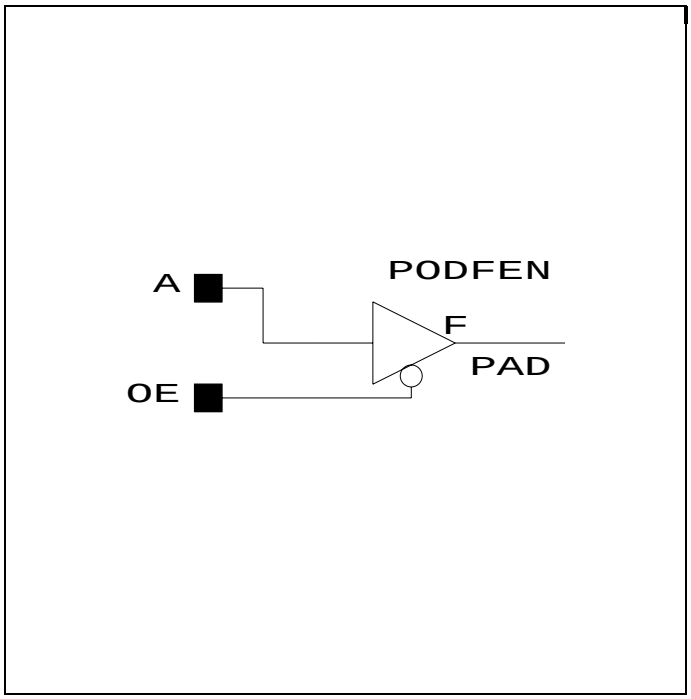
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output
OE	A	Q
1	x	w1
0	a	a

Switching Speeds for -2ns Parts

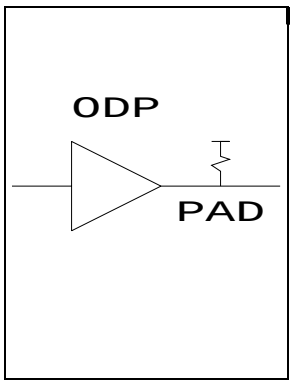
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q	2.80	4.50	7.10	3.20	4.60	7.20

ODP - Output Buffer Drive with Pull-up

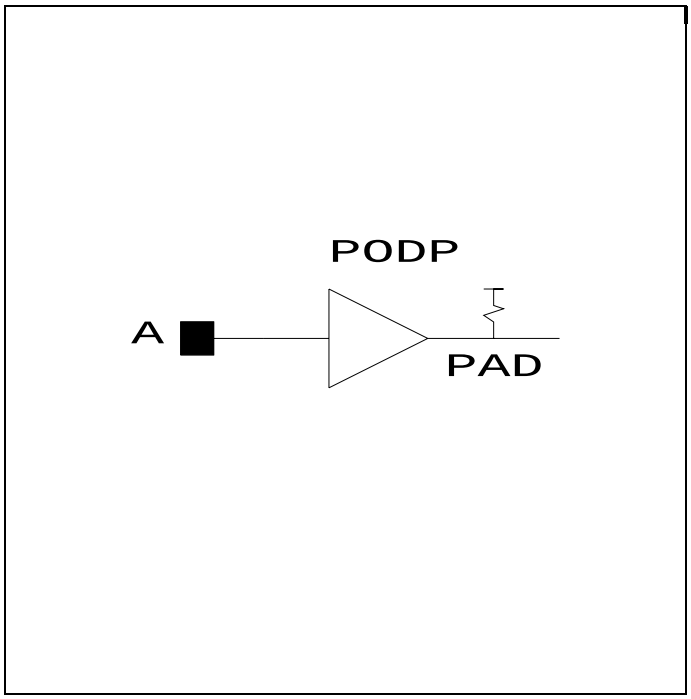
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

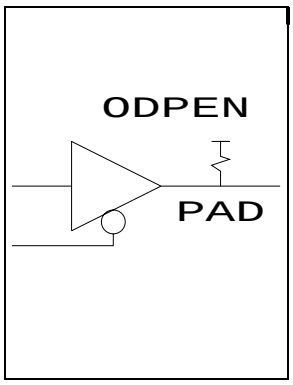
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00

ODPEN - Tristate Output with Pull-up

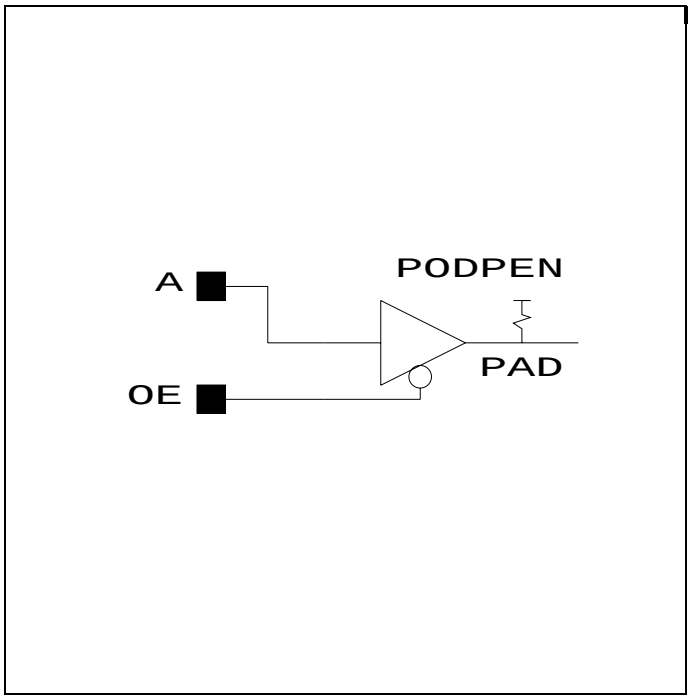
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output
OE	A	Q
1	x	z
0	a	a

Switching Speeds for -2ns Parts

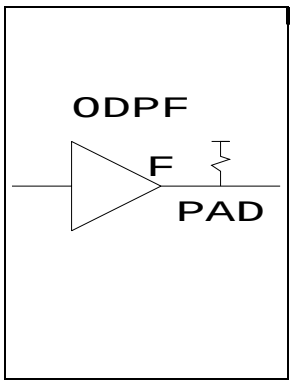
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q	5.60	7.50	11.00	7.20	9.40	13.50

ODPF - Output Buffer Drive with Fast Pull-up

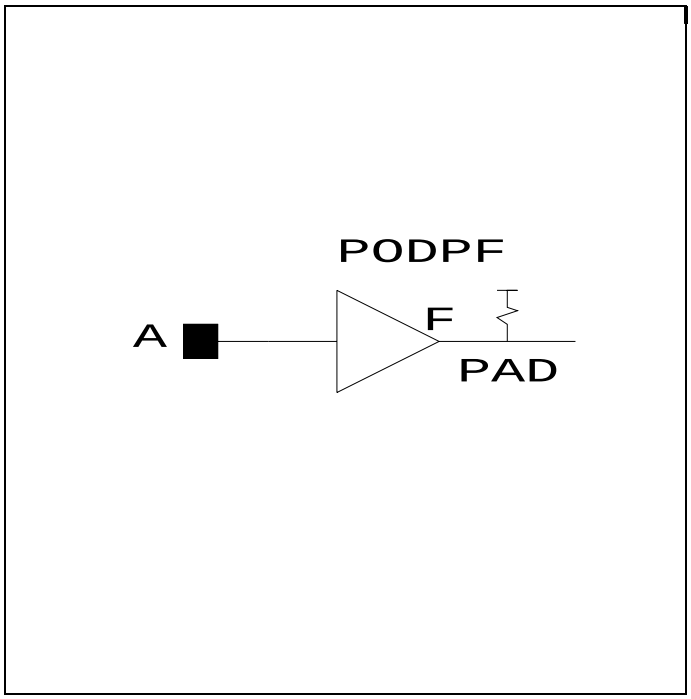
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
a	a

Switching Speeds for -2ns Parts

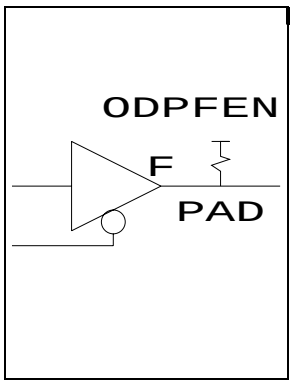
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70

ODPFEN - Tristate Output with Fast Pull-up

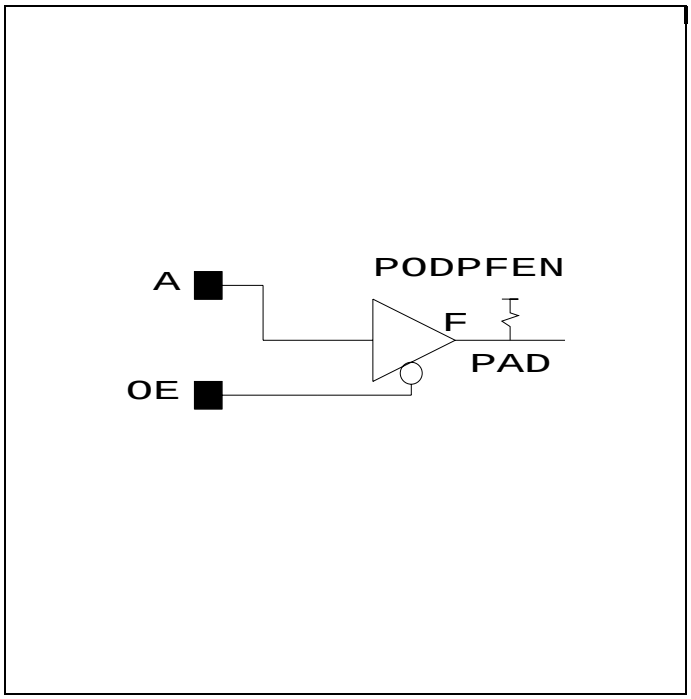
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output
OE	A	Q
1	x	w1
0	a	a

Switching Speeds for -2ns Parts

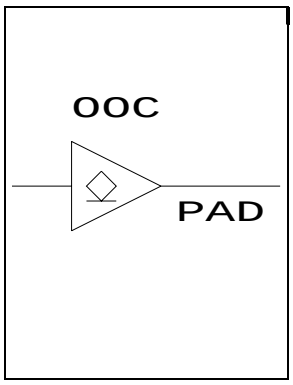
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q	2.80	4.50	7.10	3.20	4.60	7.20

OOC - Output Buffer Open Collector

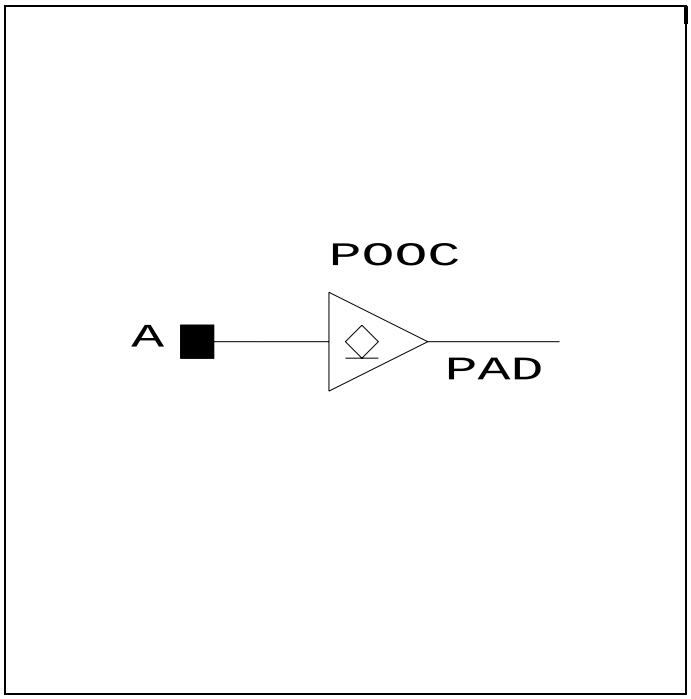
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
0	0
1	z

Switching Speeds for -2ns Parts

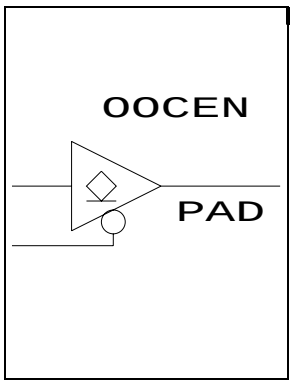
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00

OOCEN - Tristate Output Open Collector

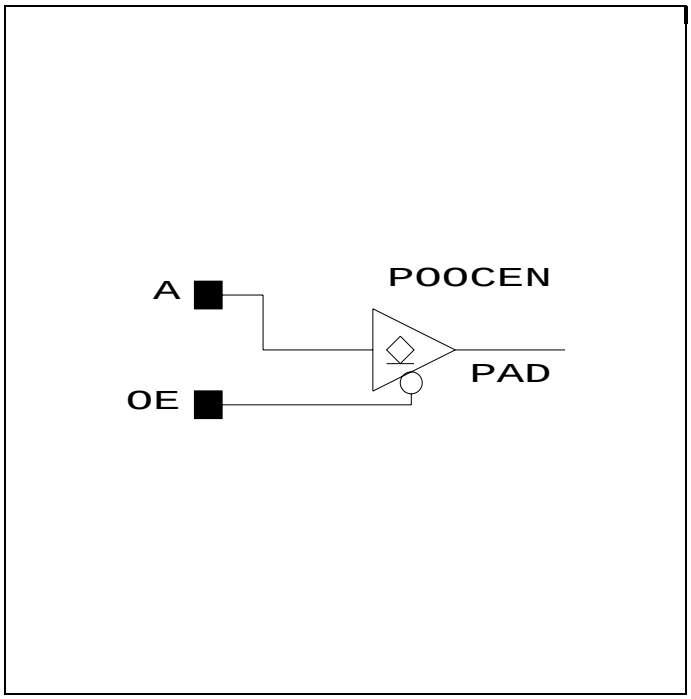
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input OE	A	Output Q
1	x	z
0	0	0
0	1	z

Switching Speeds for -2ns Parts

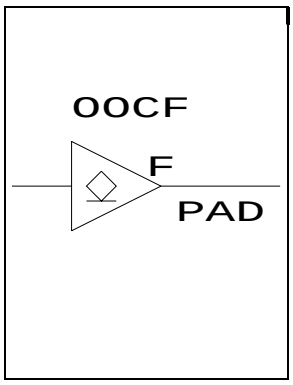
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q	5.60	7.50	11.00	7.20	9.40	13.50

OOCF - Output Buffer Open Collector Fast

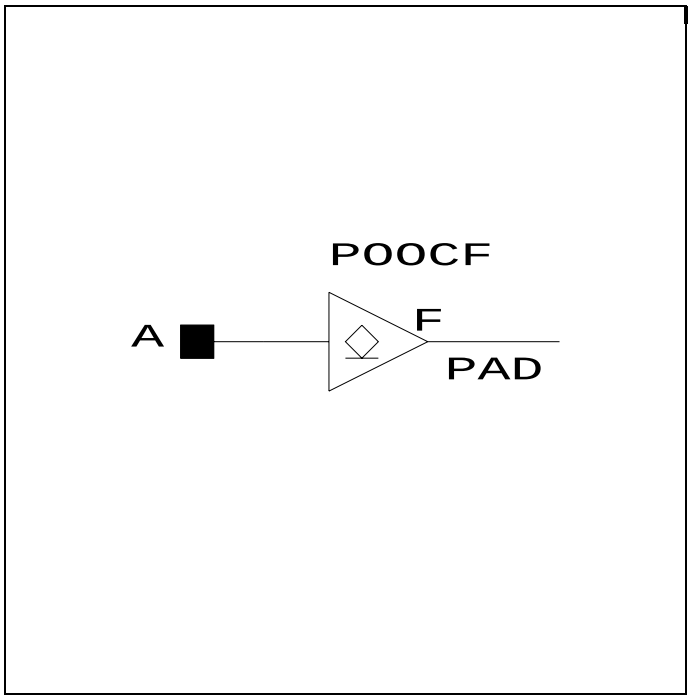
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
0	0
1	z

Switching Speeds for -2ns Parts

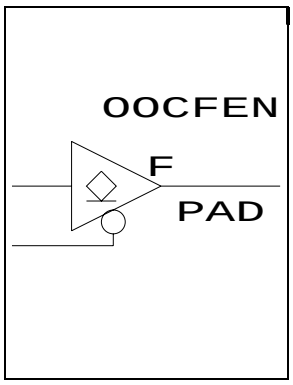
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70

OOCFEN - Tristate Output Open Collector Fast

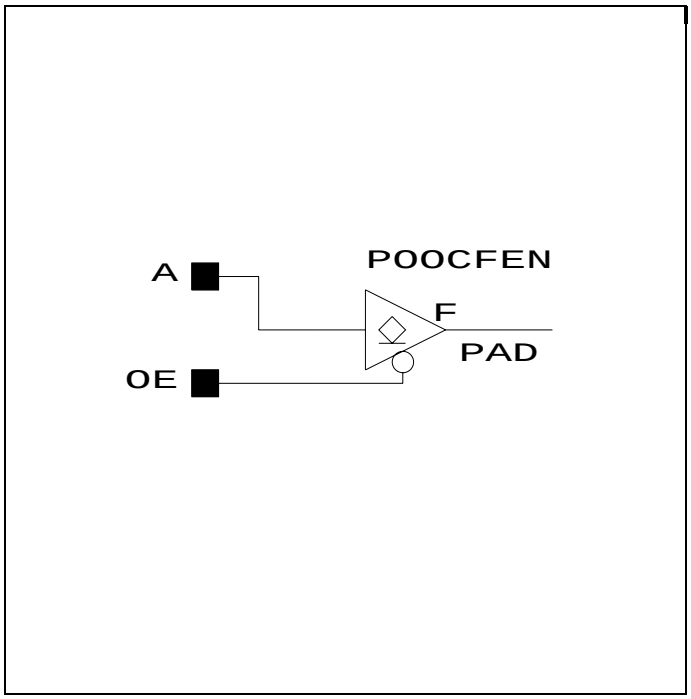
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input OE	A	Output Q
1	x	z
0	0	0
0	1	z

Switching Speeds for -2ns Parts

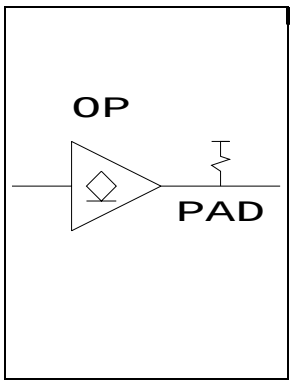
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q	2.80	4.50	7.10	3.20	4.60	7.20

OP - Output Buffer Open Coll w/ Pull-up

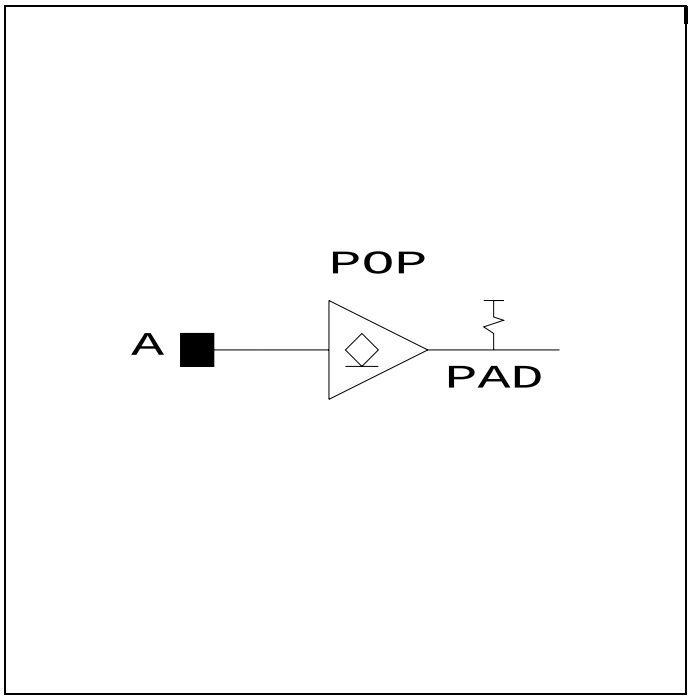
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
0	0
1	w1

*w1 = weak logical "1"

Switching Speeds for -2ns Parts

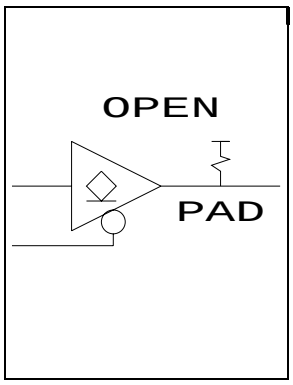
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00

OPEN/OPENB - Tristate Output Open Coll w/ Pull-up

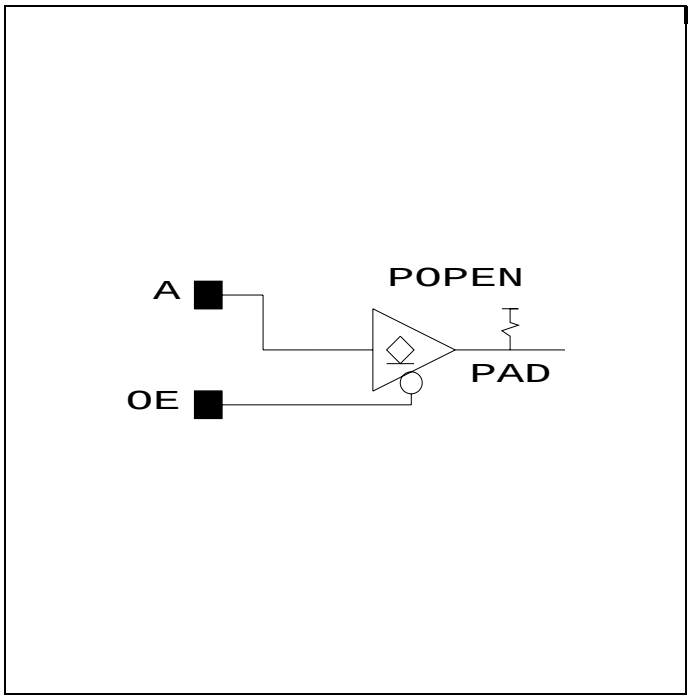
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input OE	Input A	Output Q
1	x	z
0	0	0
0	1	w1

*w1 = weak logical "1"

Switching Speeds for -2ns Parts

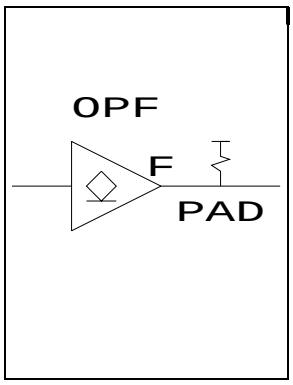
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	2.70	5.50	8.70	4.10	6.80	9.90
OE → Q	2.40	5.20	8.40	3.80	6.50	9.60

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	6.10	8.00	11.60	7.60	9.90	14.00
OE → Q	5.60	7.50	11.00	7.20	9.40	13.50

OPF - Output Buffer Open Coll w/ Fast Pull-up

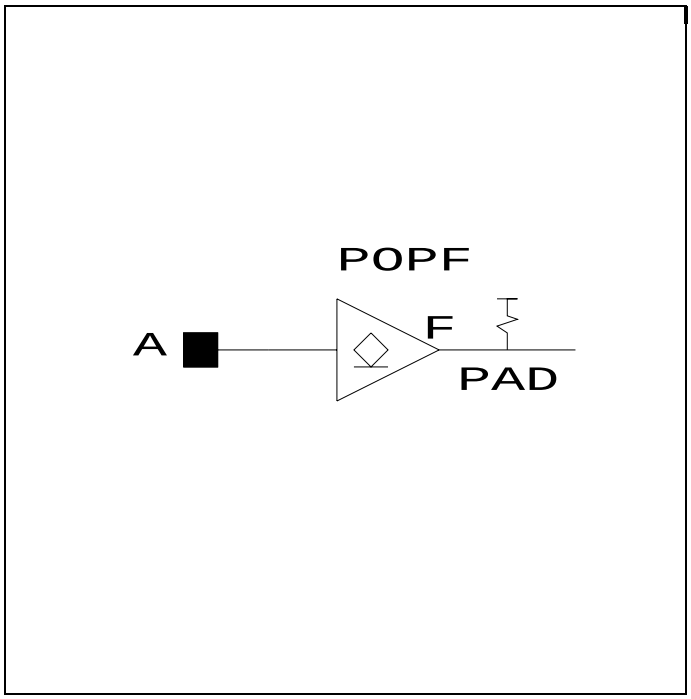
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
0	0
1	w1

*w1 = weak logical "1"

Switching Speeds for -2ns Parts

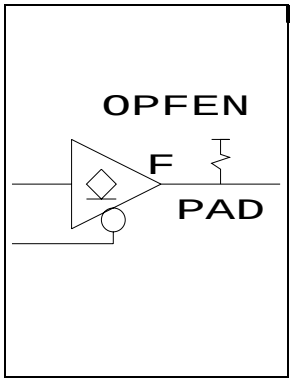
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70

OPFEN - Tristate Open Collector w/ Fast Pull-up

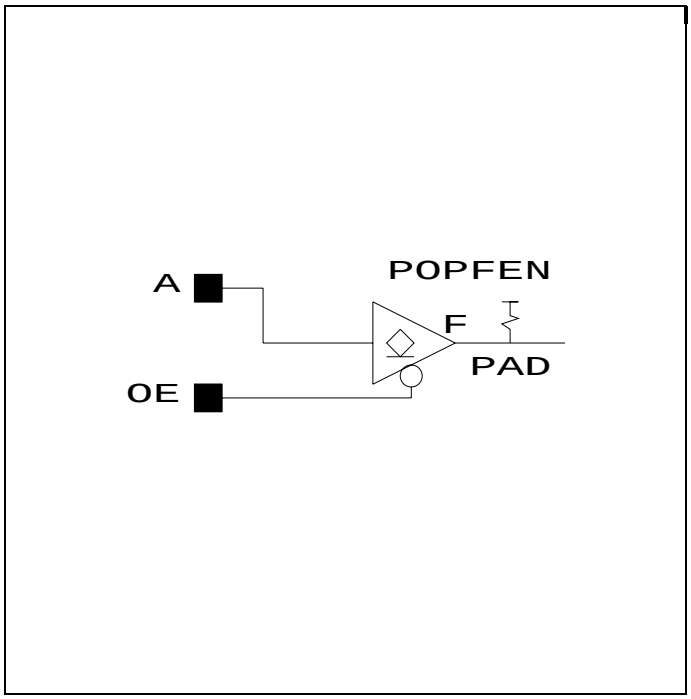
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output
OE	A	Q
1	x	z
0	0	0
0	1	w1

*w1 = weak logical "1"

Switching Speeds for -2ns Parts

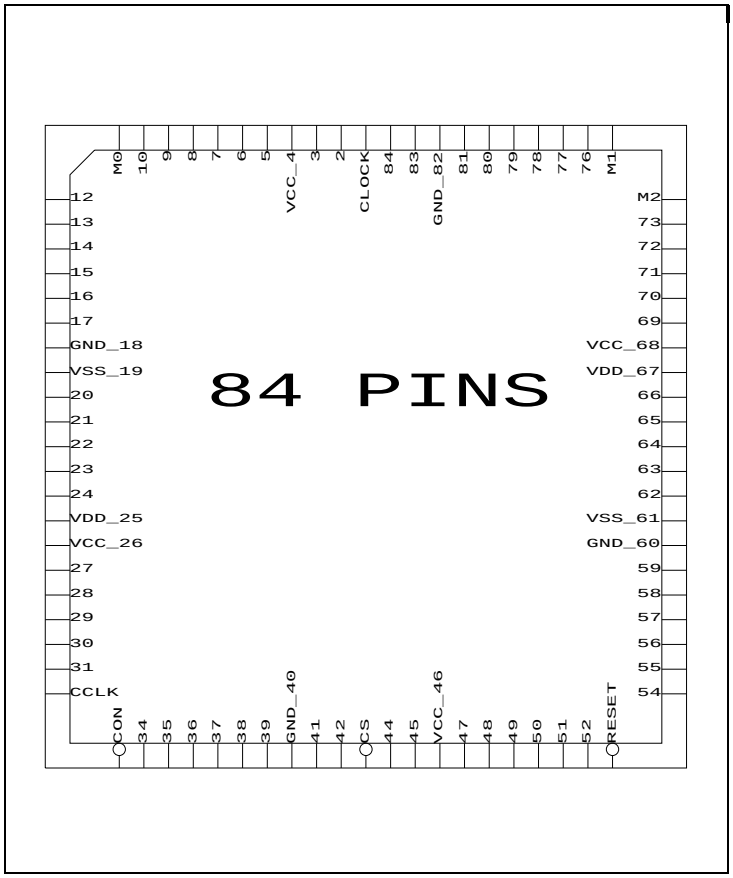
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.50	2.90	5.50	1.90	3.20	5.50
OE → Q	1.20	2.60	5.20	1.60	2.80	5.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.30	5.00	7.60	3.60	5.10	7.70
OE → Q	2.80	4.50	7.10	3.20	4.60	7.20

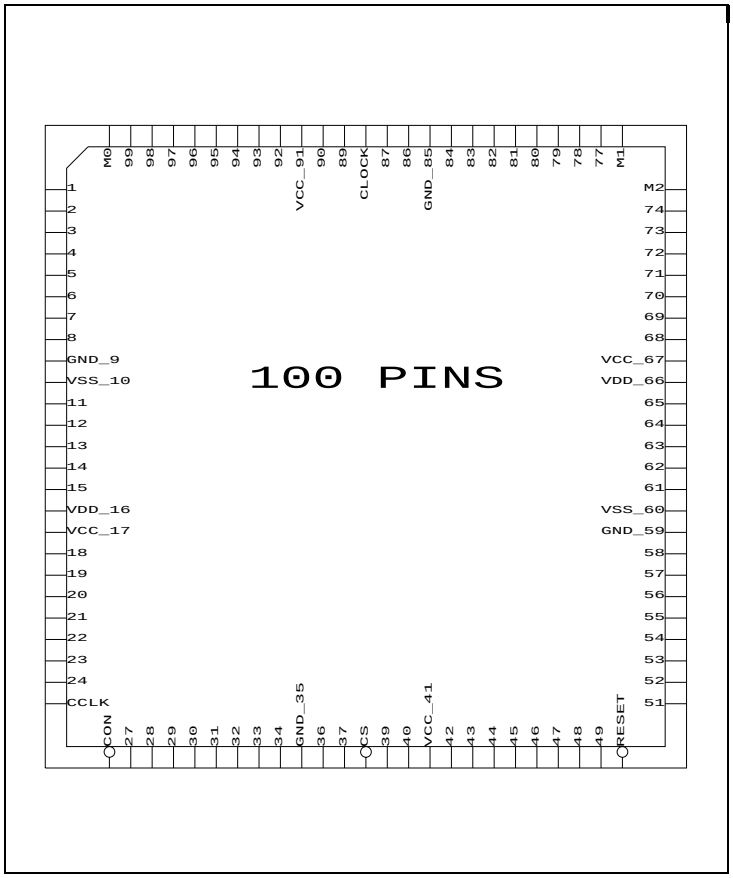
PLCC84 - 84 Pin PLCC Package

Symbol



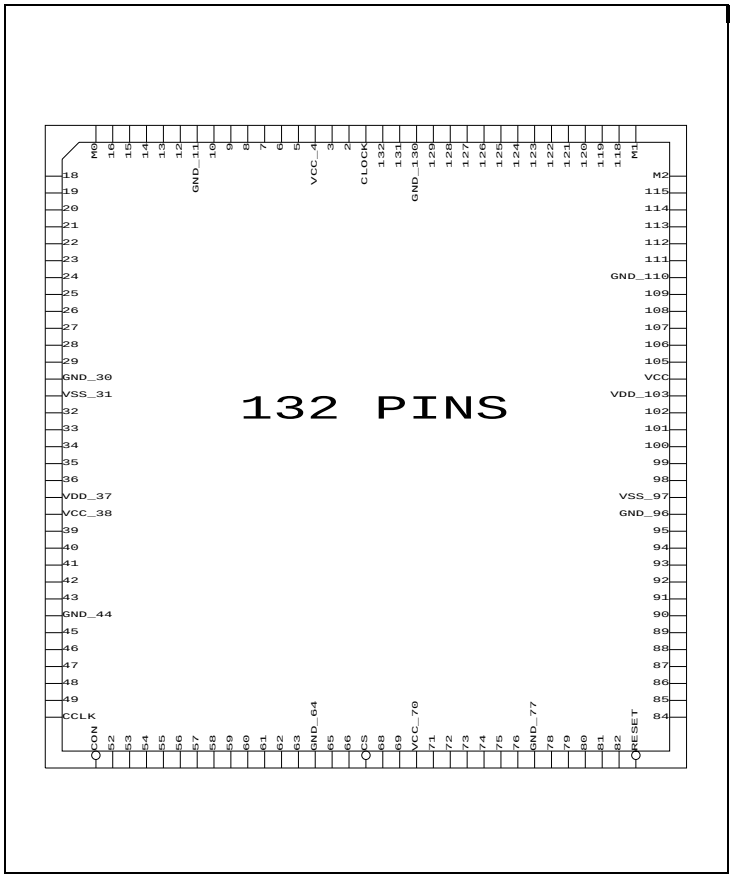
PQFP100 - 100 Pin PQFP Package

Symbol



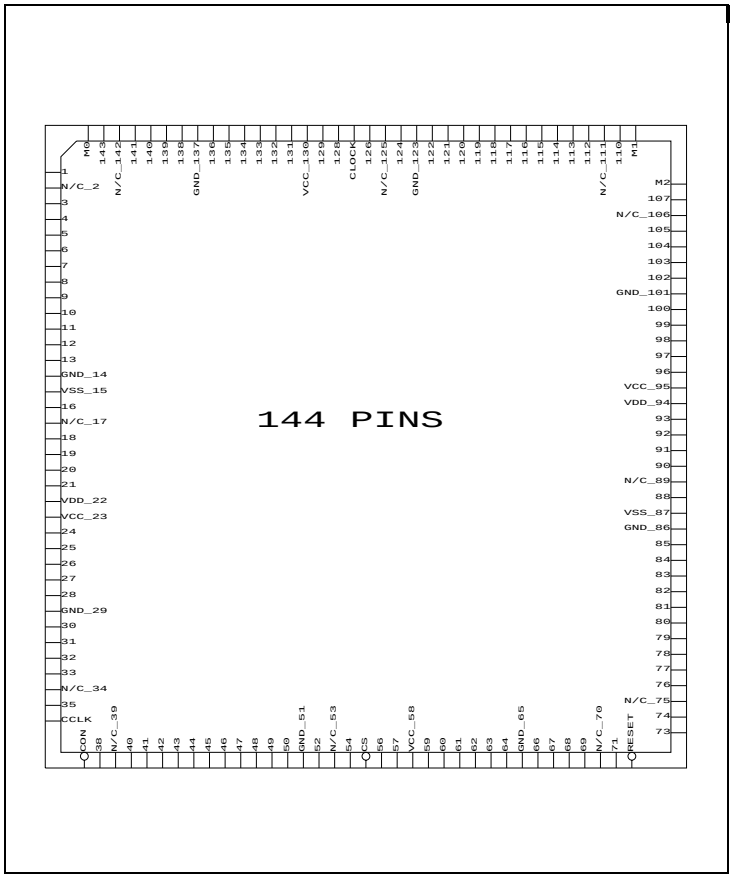
PQFP132 - 132 Pin PQFP Package

Symbol



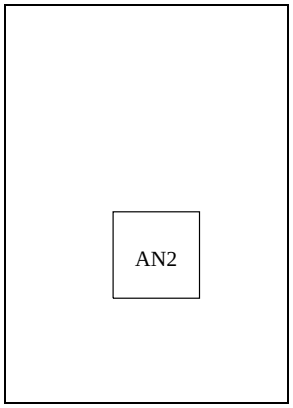
PQFP144 - 144 Pin PQFP Package

Symbol



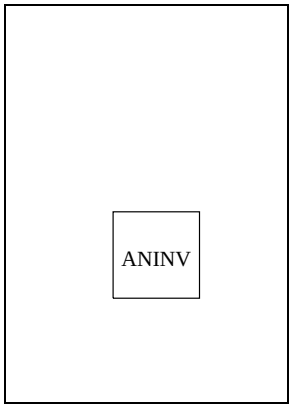
AN2 - 2-Input AND

Layout for Shape 1



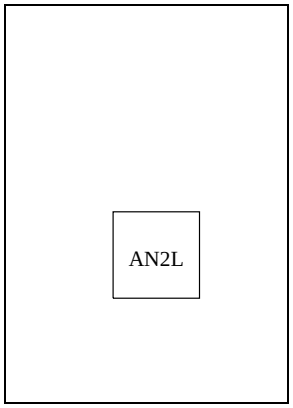
AN2INV - 2-Input AND with Inverted Input (A*B')

Layout for Shape 1



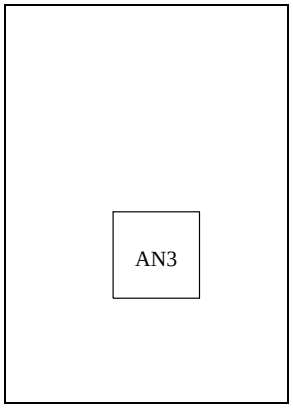
AN2L - 2-Input AND (AB')

Layout for Shape 1, Default



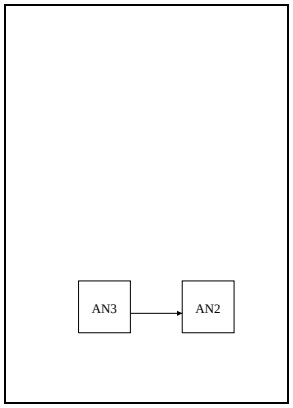
AN3 - 3-Input AND

Layout for Shape 1, Default



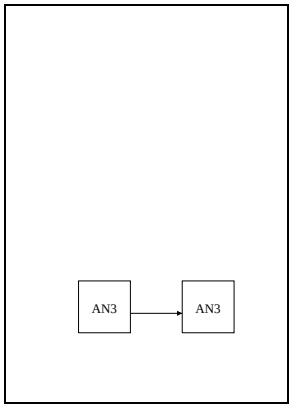
AN4 - 4-Input AND

Layout for Shape 1, Default



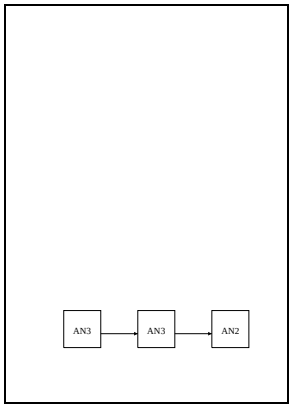
AN5 - 5-Input AND

Layout for Shape 1, Default



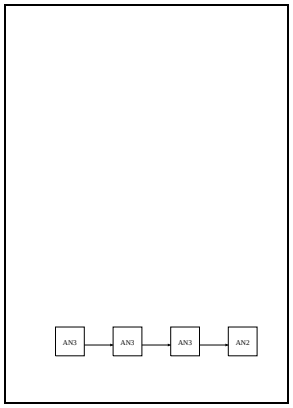
AN6 - 6-Input AND

Layout for Shape 1, Default



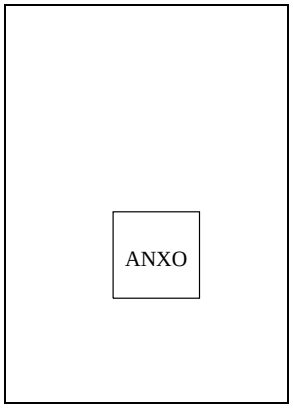
AN8 - 8-Input AND

Layout for Shape 1, Default



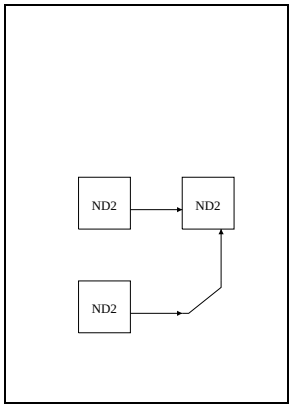
ANXO - 2-Input AND Feeding an XOR

Layout for Shape 1



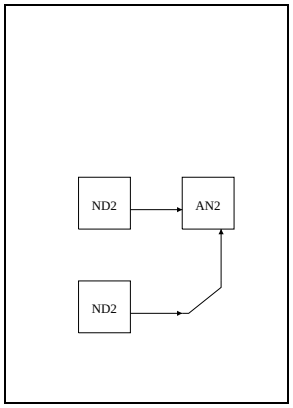
AO22 - AND-OR Inverter 2-2 Inputs

Layout for Shape 1



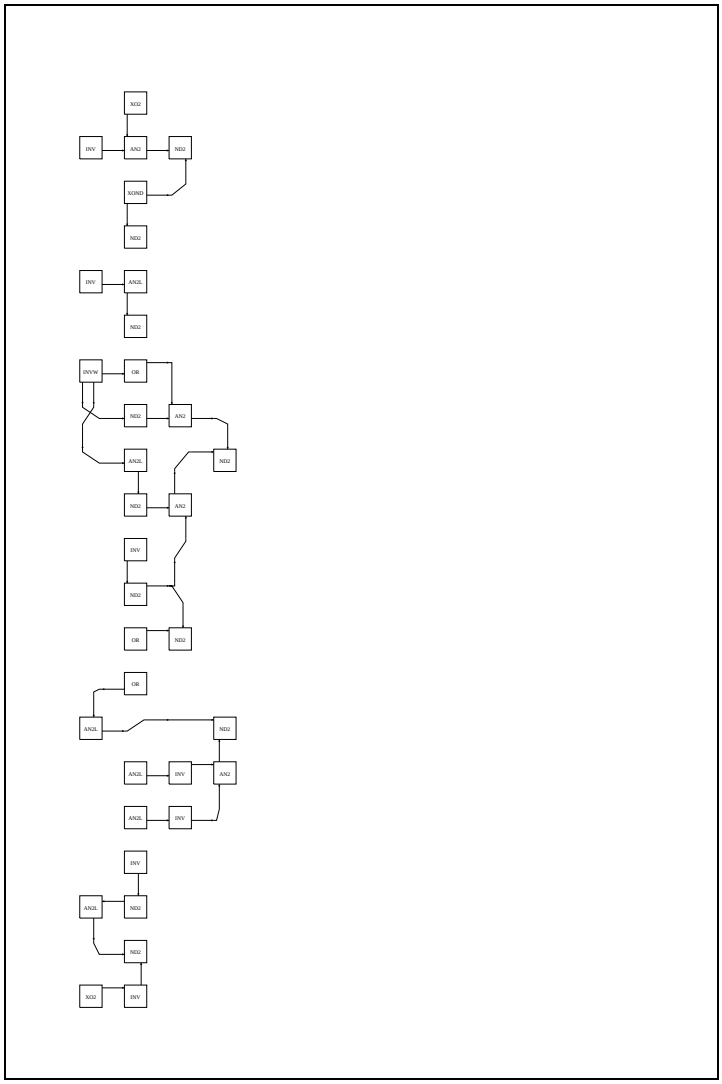
AOI22 - AND-OR Inverter 2-2 Inputs

Layout for Shape 1



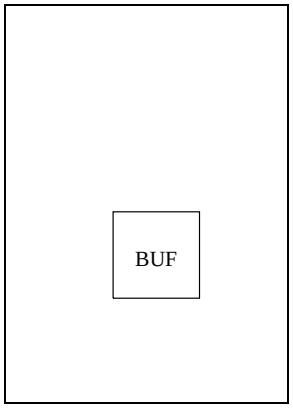
BCD7SEG - 7-Segment BCD Display (0 to 9)

Layout for Shape 1



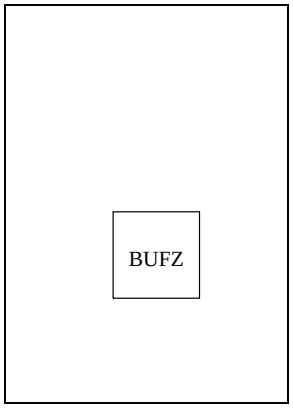
BUFFER/BUFFERB - Buffer

Layout for Shape 1



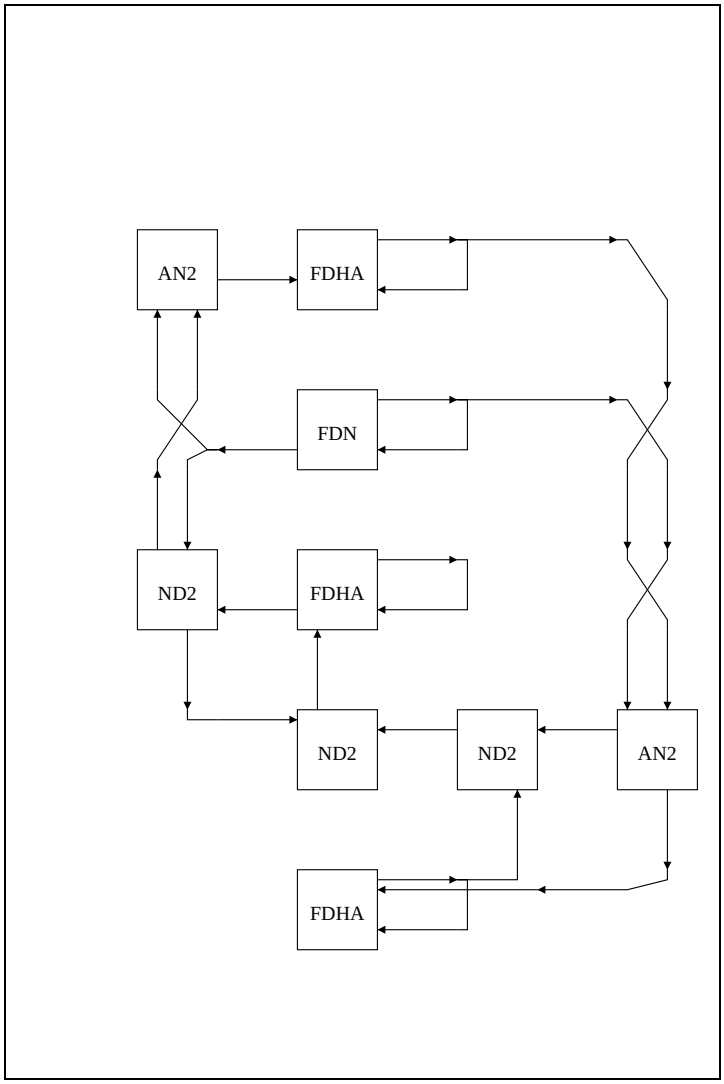
BUFZ - Tristate Buffer

Layout for Shape 1



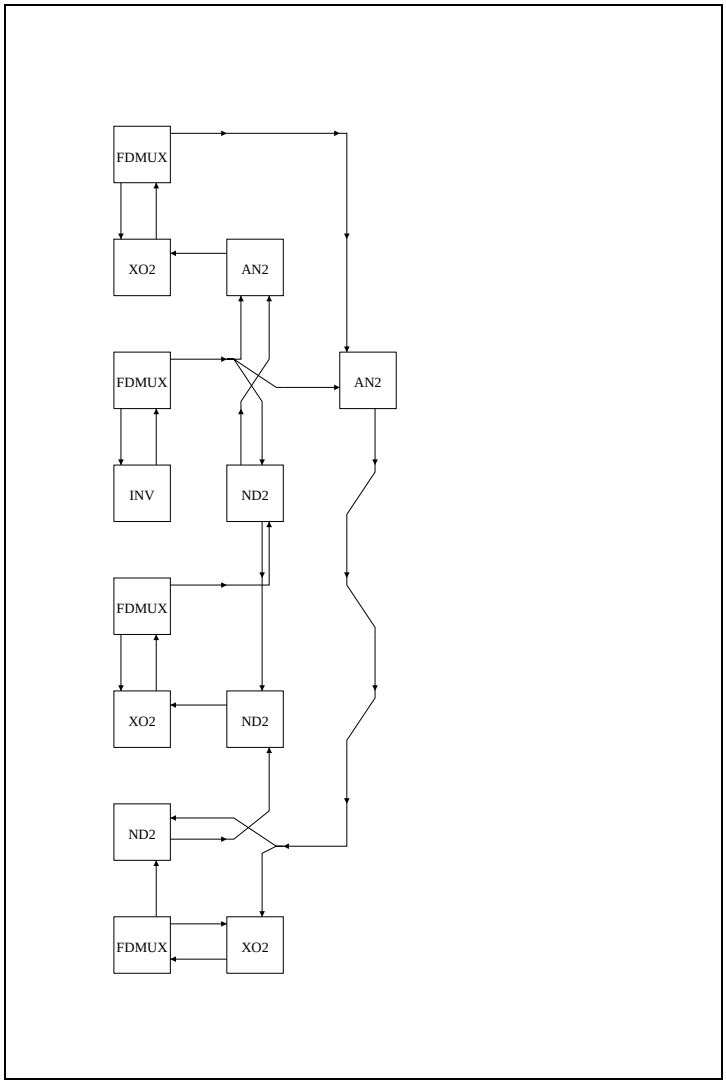
CD4 - 4-Bit Decade Counter

Layout for Shape 1



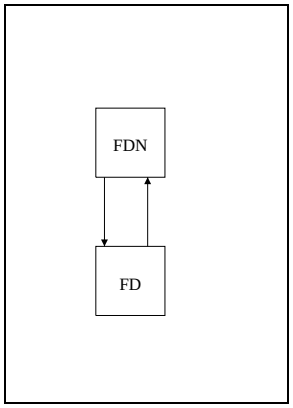
CDP4 - 4-Bit Decade Counter w/ Parallel Load

Layout for Shape 1



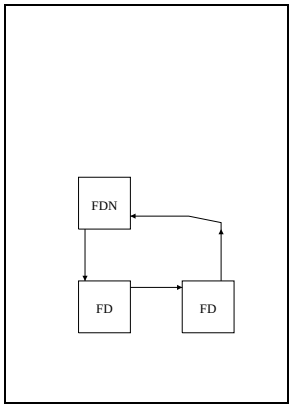
CJ2 - 2-Bit Johnson Counter

Layout for Shape 1



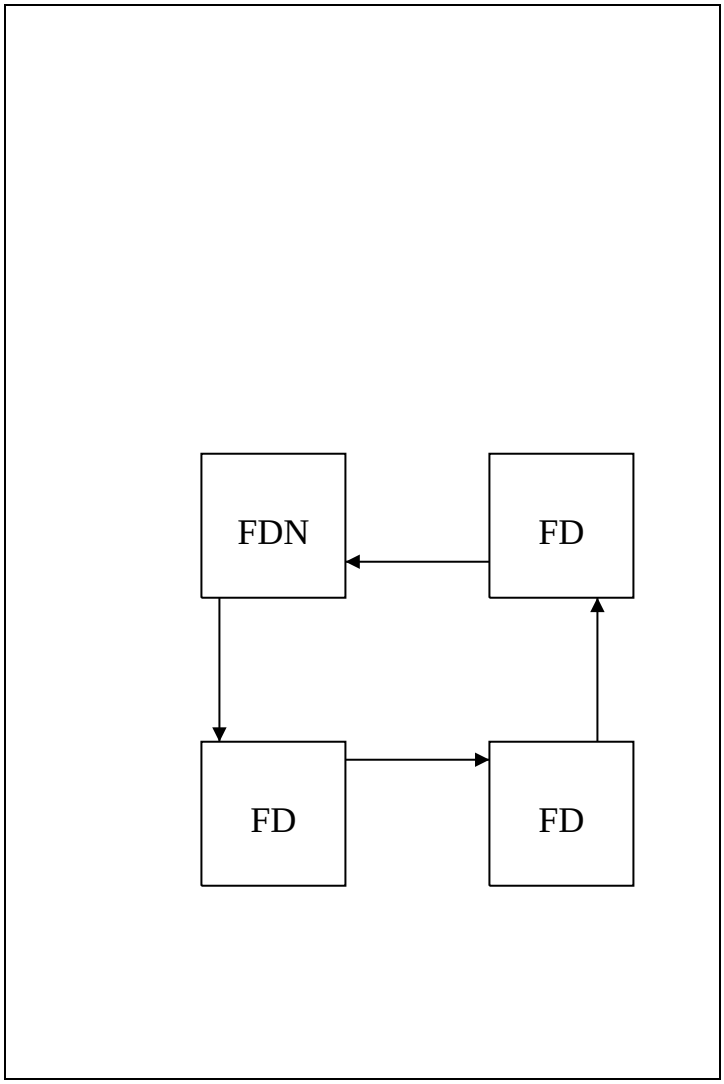
CJ3 - 3-Bit Johnson Counter

Layout for Shape 1



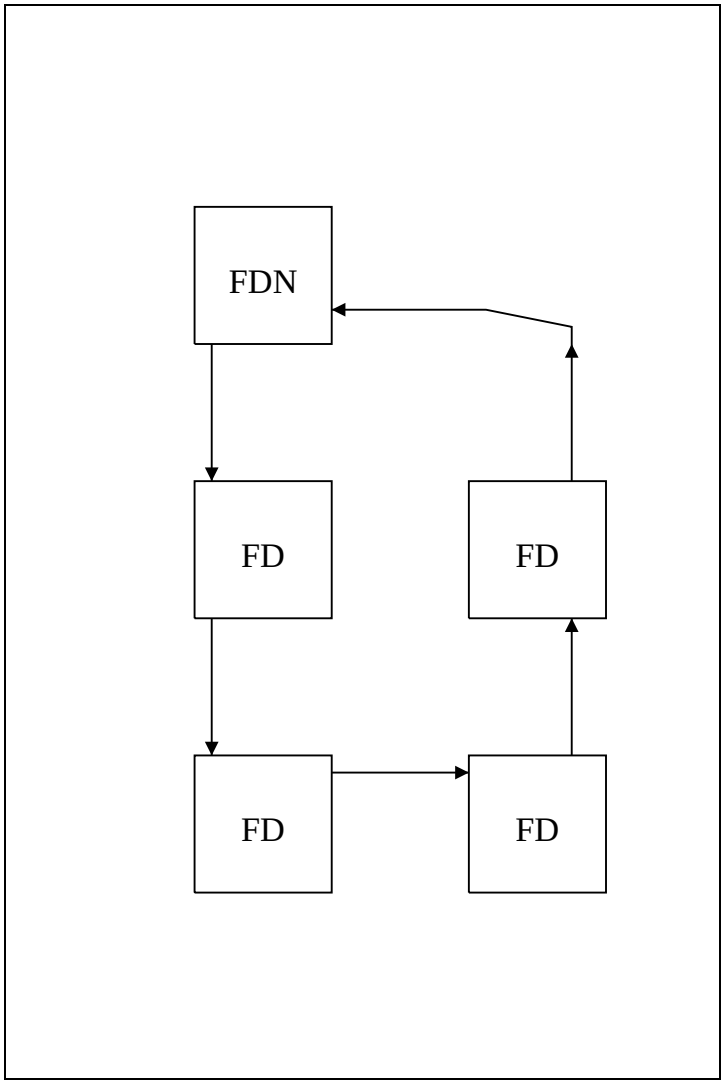
CJ4 - 4-Bit Johnson Counter

Layout for Shape 1



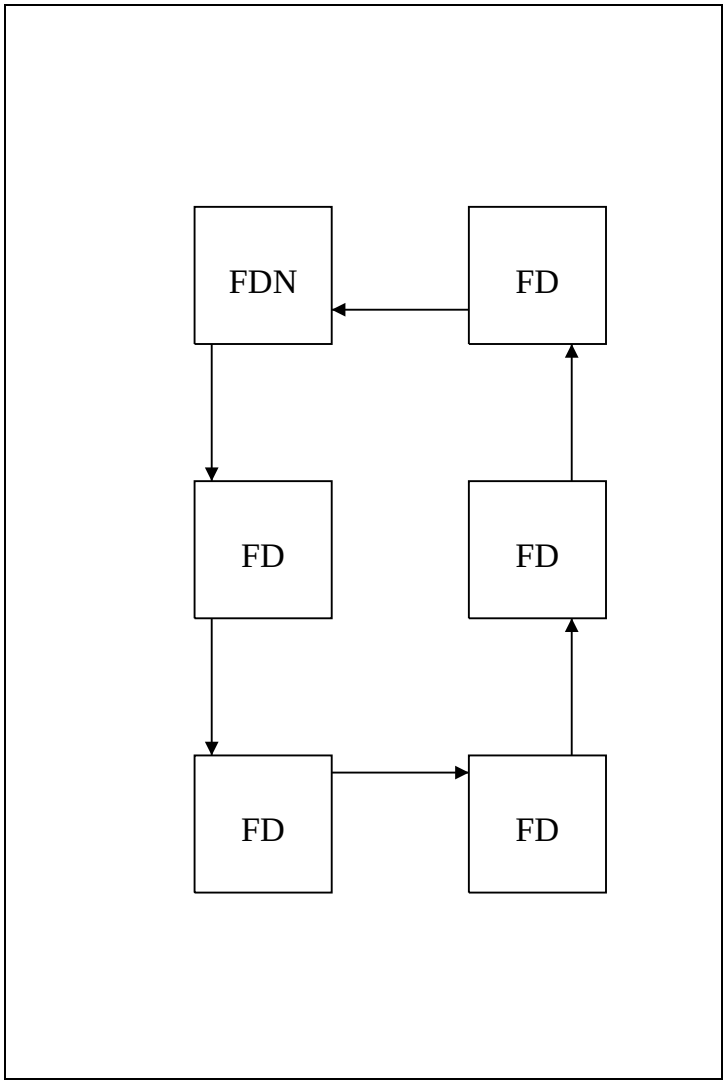
CJ5 - 5-Bit Johnson Counter

Layout for Shape 1



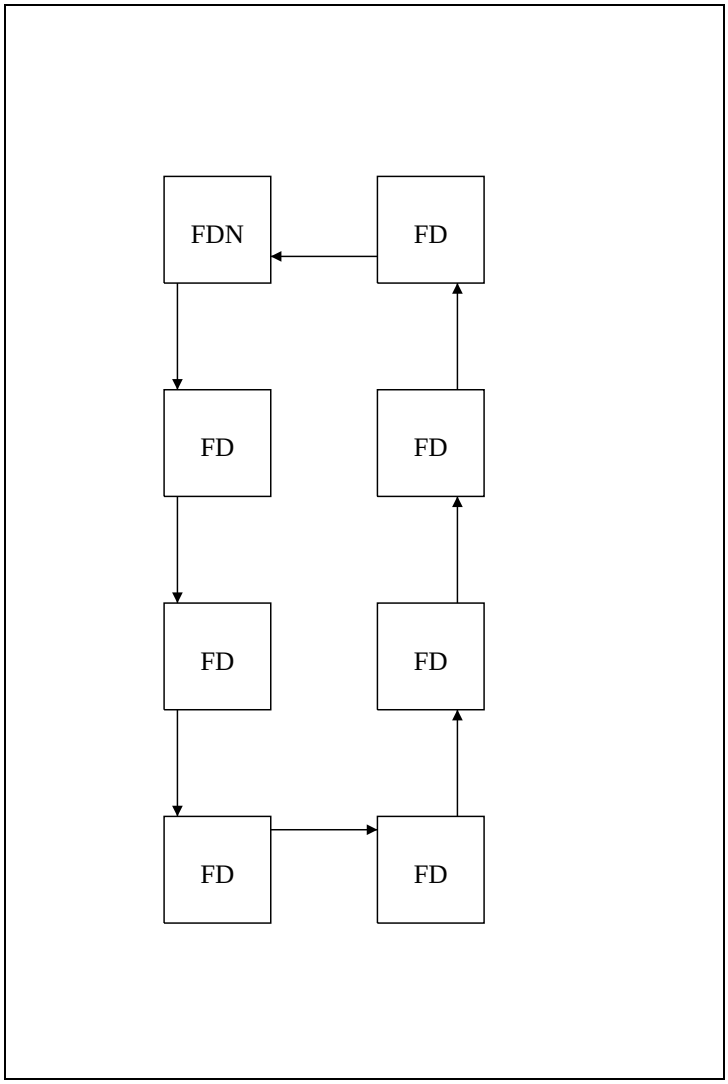
CJ6 - 6-Bit Johnson Counter

Layout for Shape 1



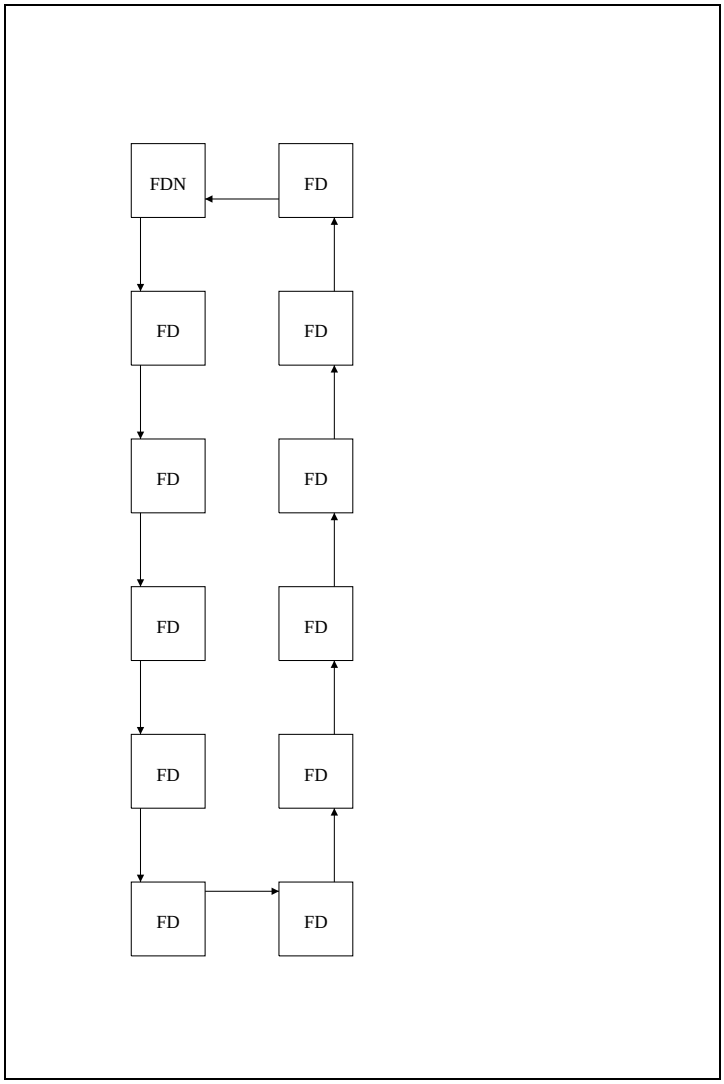
CJ8 - 8-Bit Johnson Counter

Layout for Shape 1



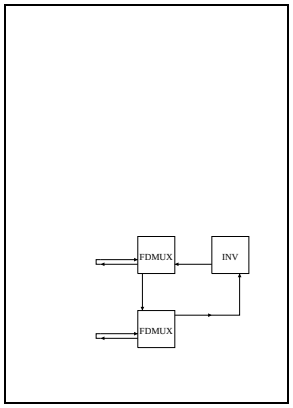
CJ12 - 12-Bit Johnson Counter

Layout for Shape 1



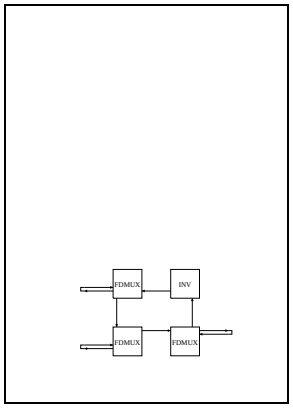
CJE2 - 2-Bit Johnson Counter with Enable

Layout for Shape 1



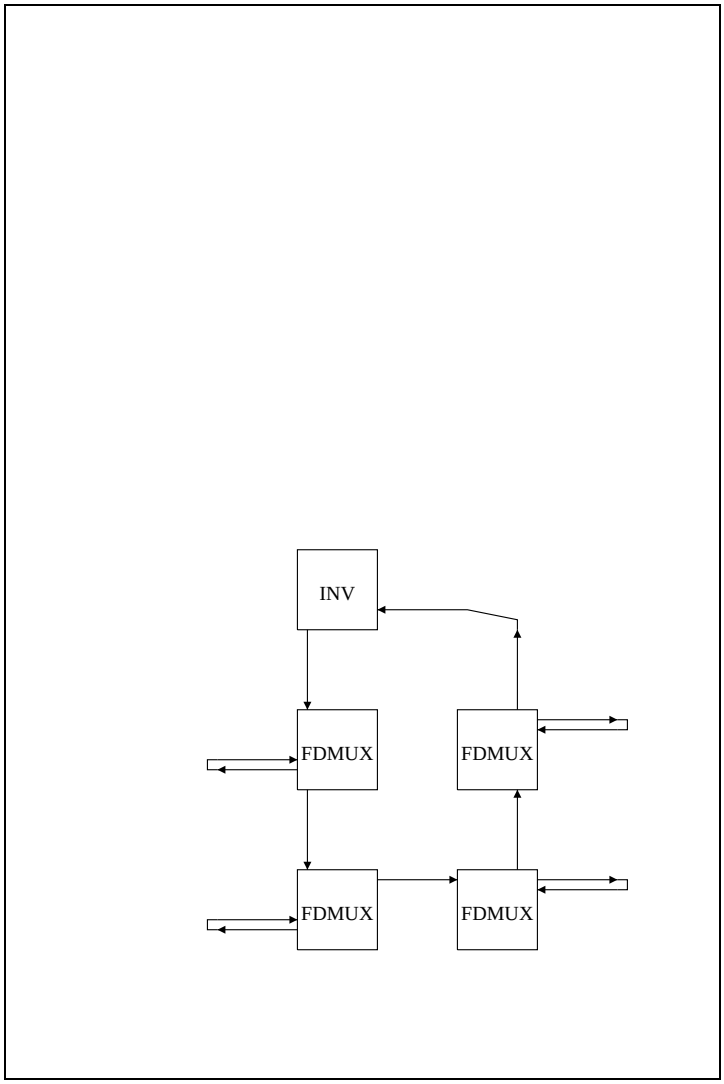
CJE3 - 3-Bit Johnson Counter with Enable

Layout for Shape 1



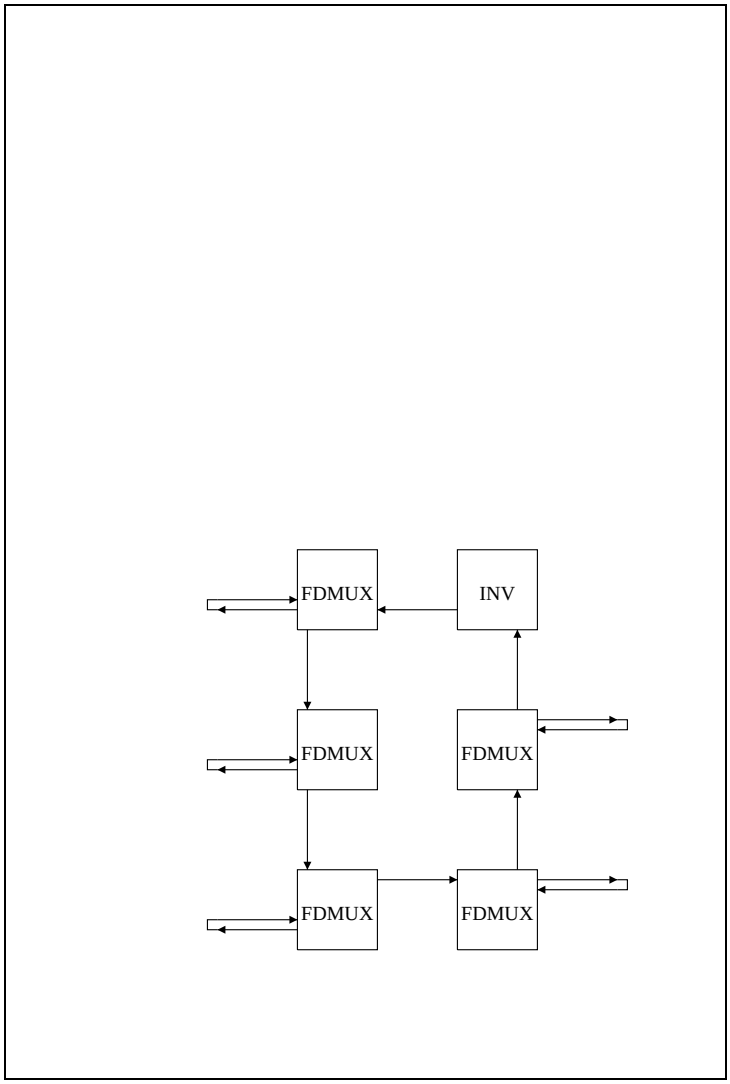
CJE4 - 4-Bit Johnson Counter with Enable

Layout for Shape 1



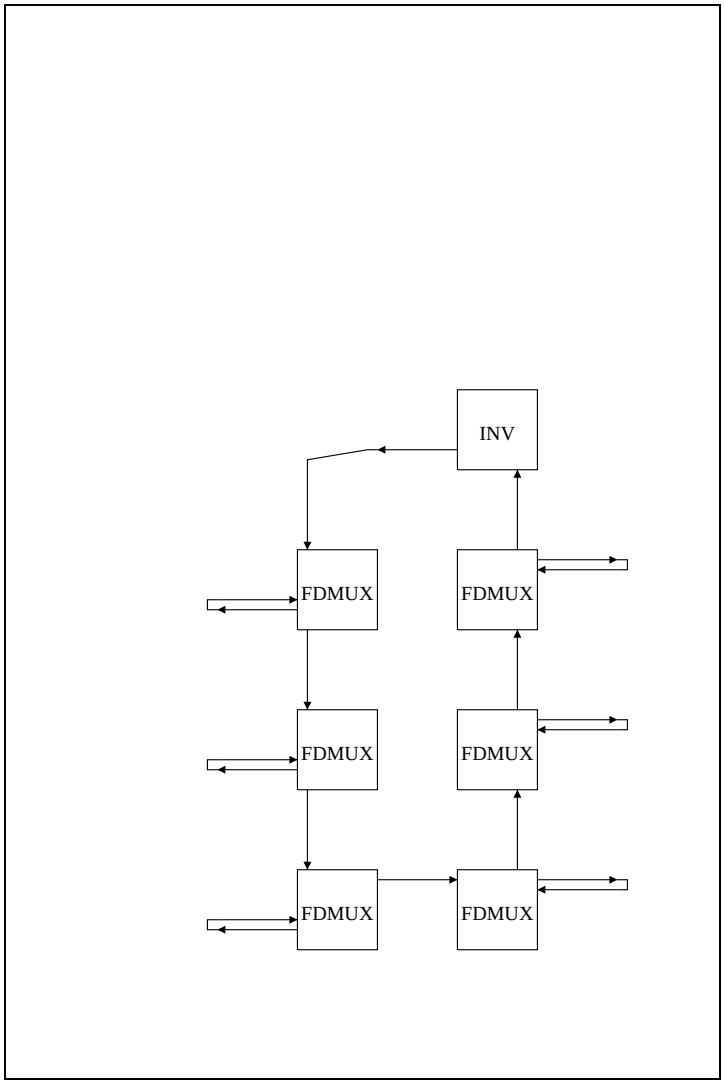
CJE5 - 5-Bit Johnson Counter with Enable

Layout for Shape 1



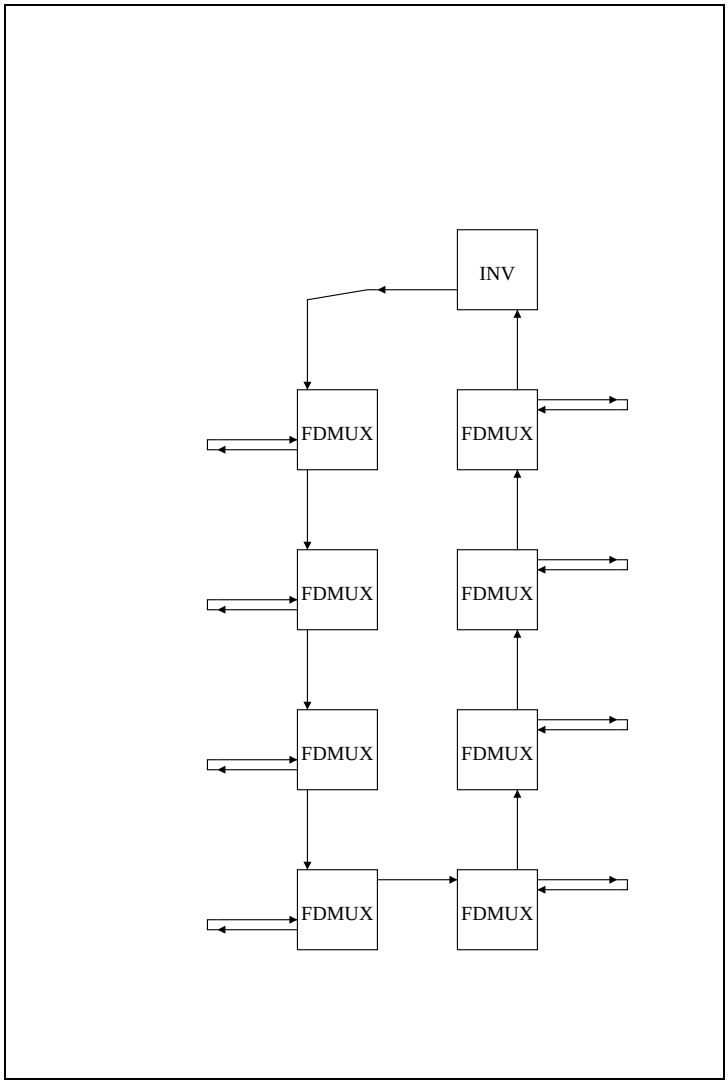
CJE6 - 6-Bit Johnson Counter with Enable

Layout for Shape 1



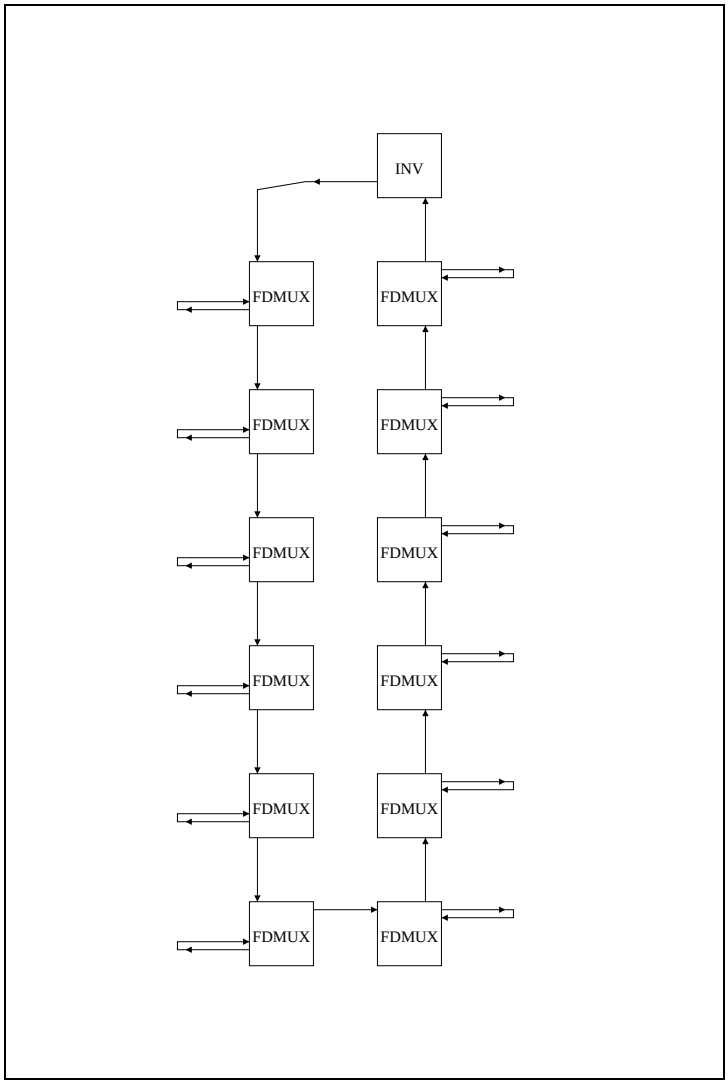
CJE8 - 8-Bit Johnson Counter with Enable

Layout for Shape 1



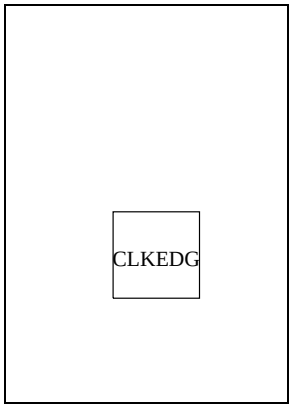
CJE12 - 12-Bit Johnson Counter with Enable

Layout for Shape 1



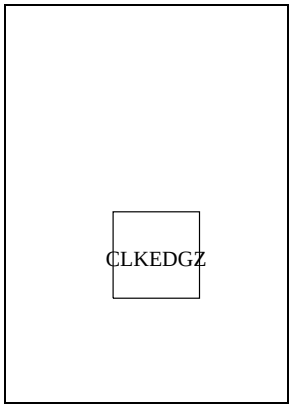
CLKEDGE - Clock Edge Detect

Layout for Shape 1



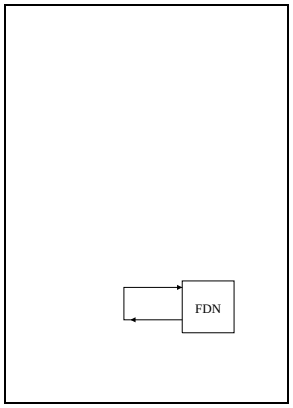
CLKEDGEZ - Clock Edge Detect Q=1 on Rise (Z)

Layout for Shape 1



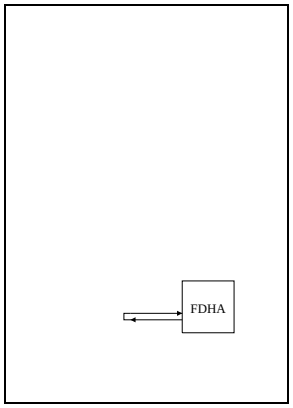
CR0 - 0-Bit Ripple-Carry Counter

Layout for Shape 1



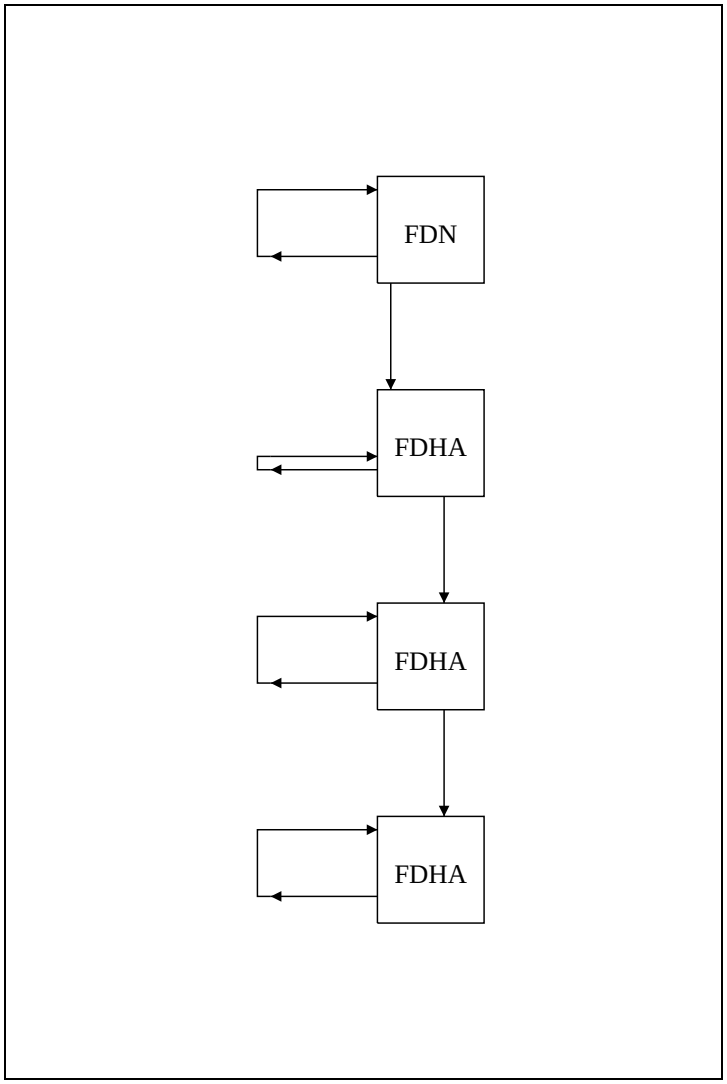
CR1 - 1-Bit Ripple-Carry Counter

Layout for Shape 1



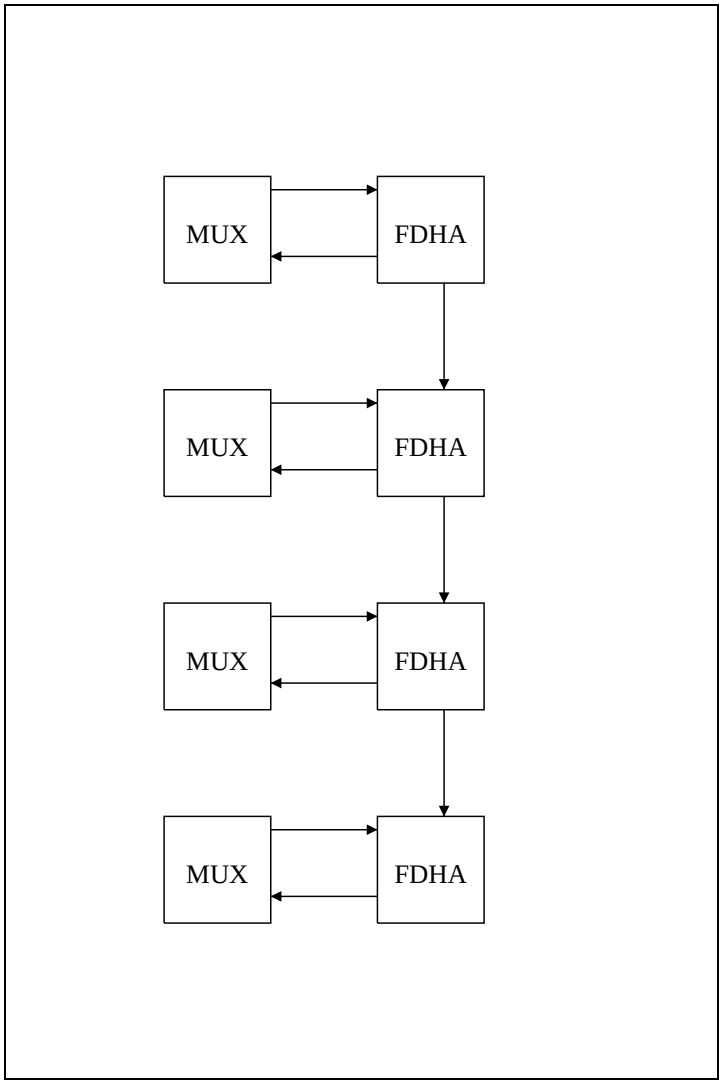
CR4 - 4-Bit Ripple-Carry Counter

Layout for Shape 1



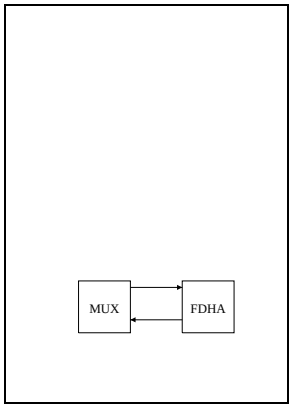
CRP4 - 4-Bit Ripple-Carry Counter w/ Parallel Load

Layout for Shape 1



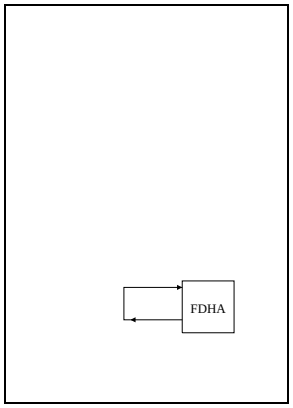
CRPST - Bit Stage Ripple-Carry w/ Parallel Load

Layout for Shape 1



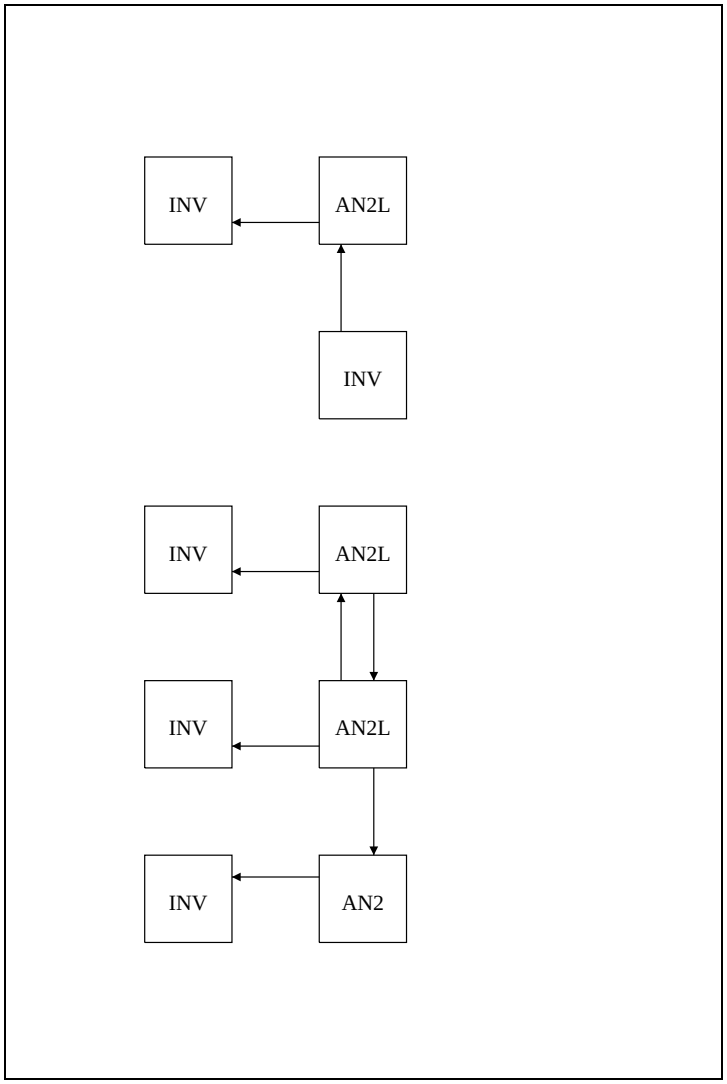
CRST - Bit Stage Ripple-Carry Counter

Layout for Shape 1



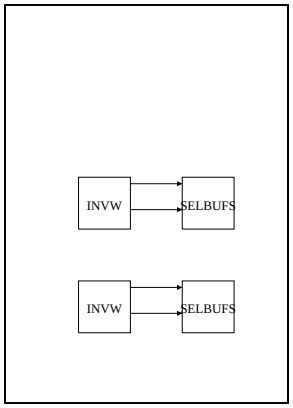
DC24 - 2-to-4 Decoder Active High/Low

Layout for Shape 1



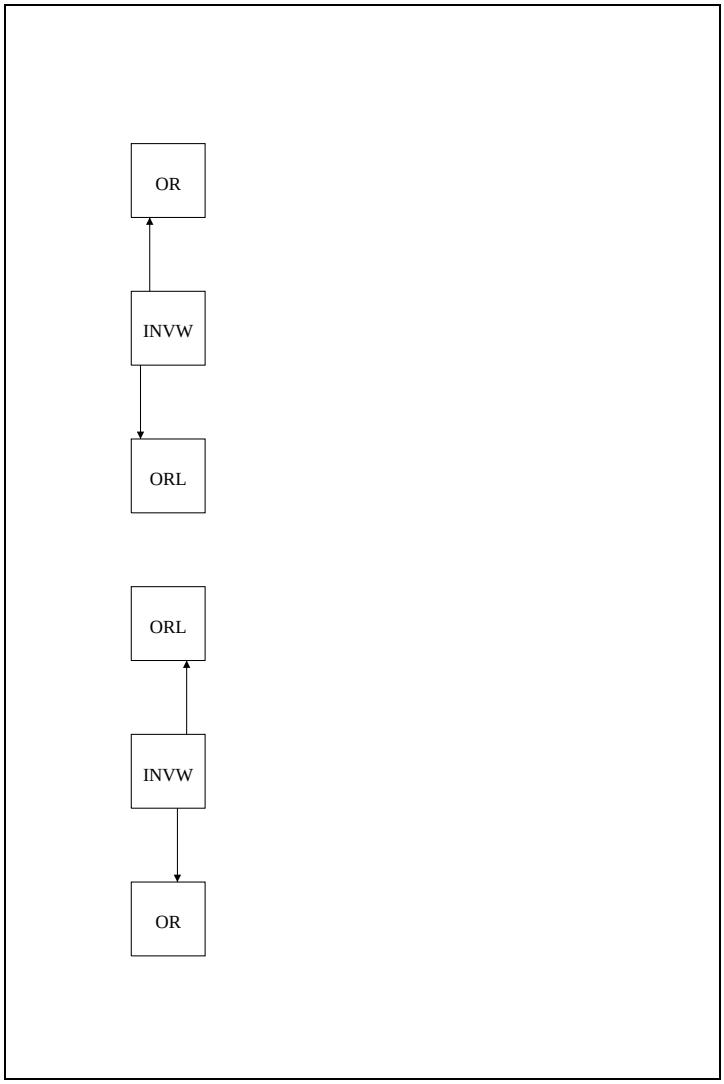
DC24H - 2-to-4 Decoder Active High

Layout for Shape 1



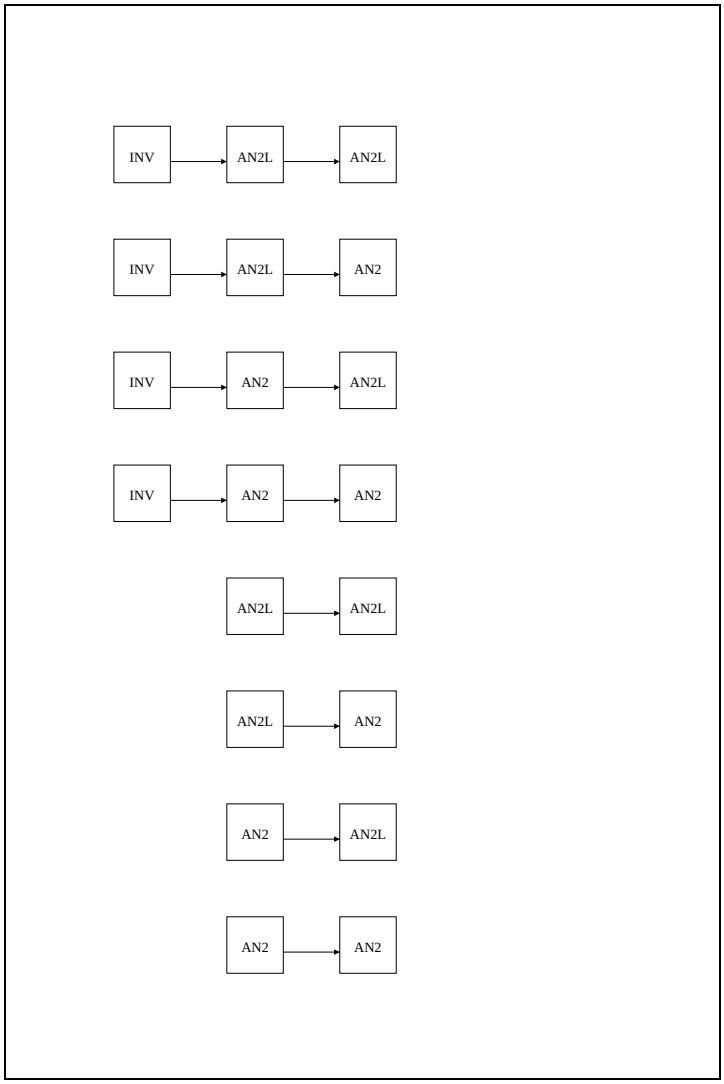
DC24L - 2-to-4 Decoder Active Low

Layout for Shape 1



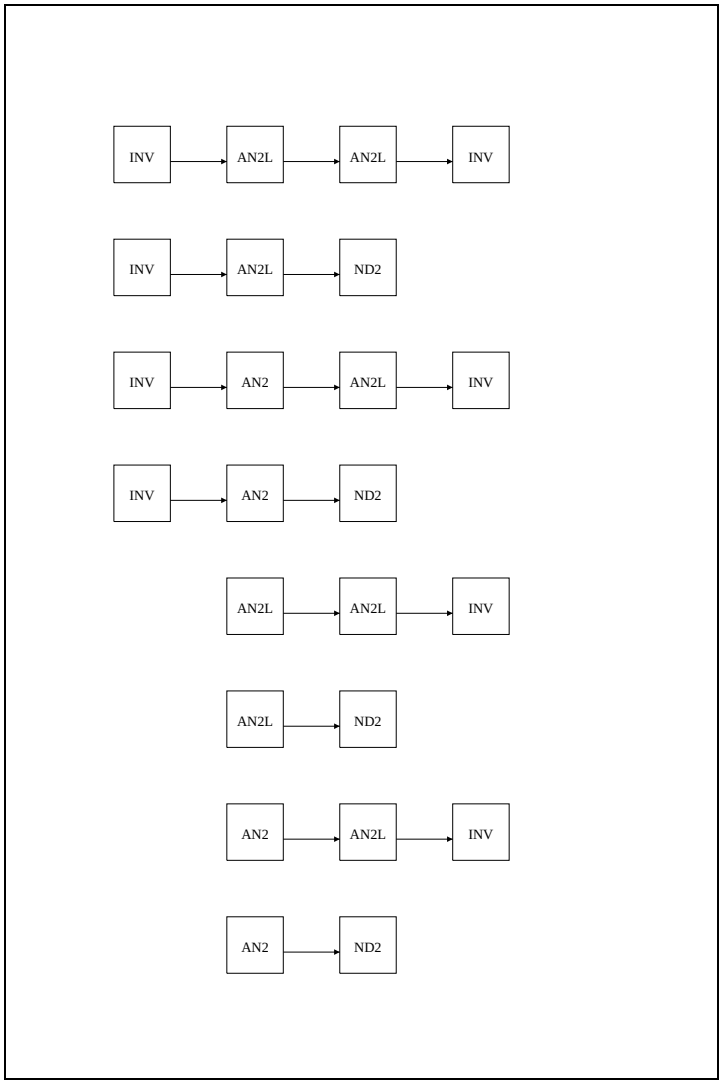
DC38H - 3-to-8 Decoder Active High

Layout for Shape 1



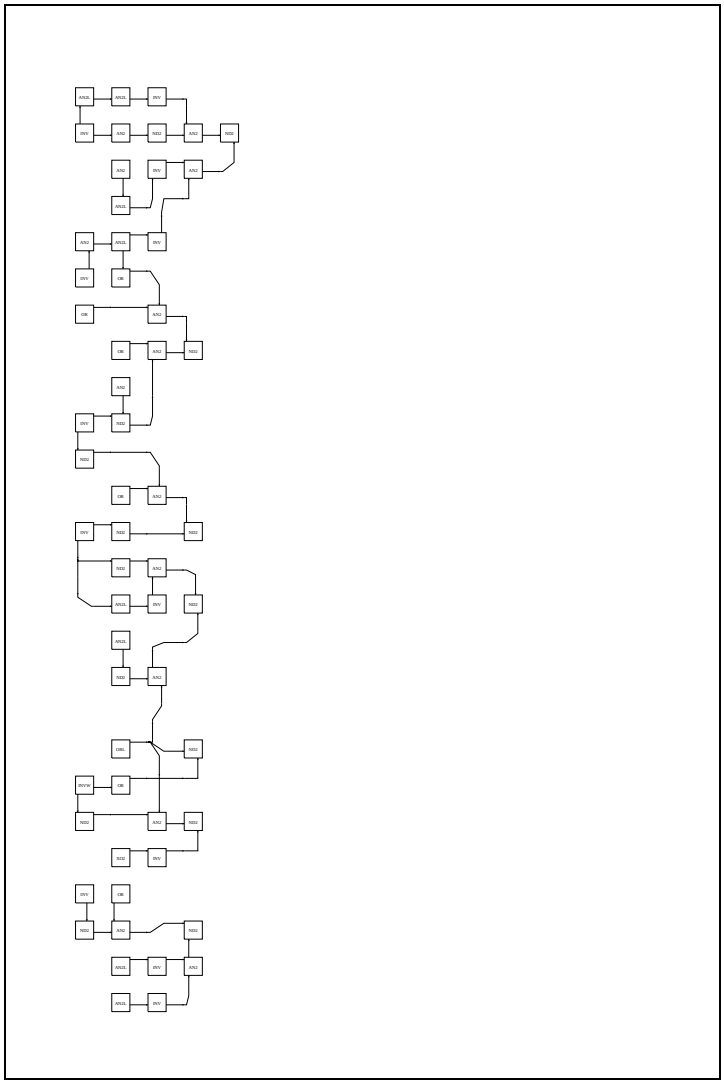
DC38L - 3-to-8 Decoder Active Low

Layout for Shape 1



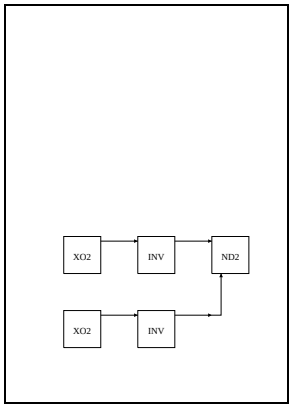
DIS7SEG - 7 Segment BCD Display (0 to F)

Layout for Shape 1



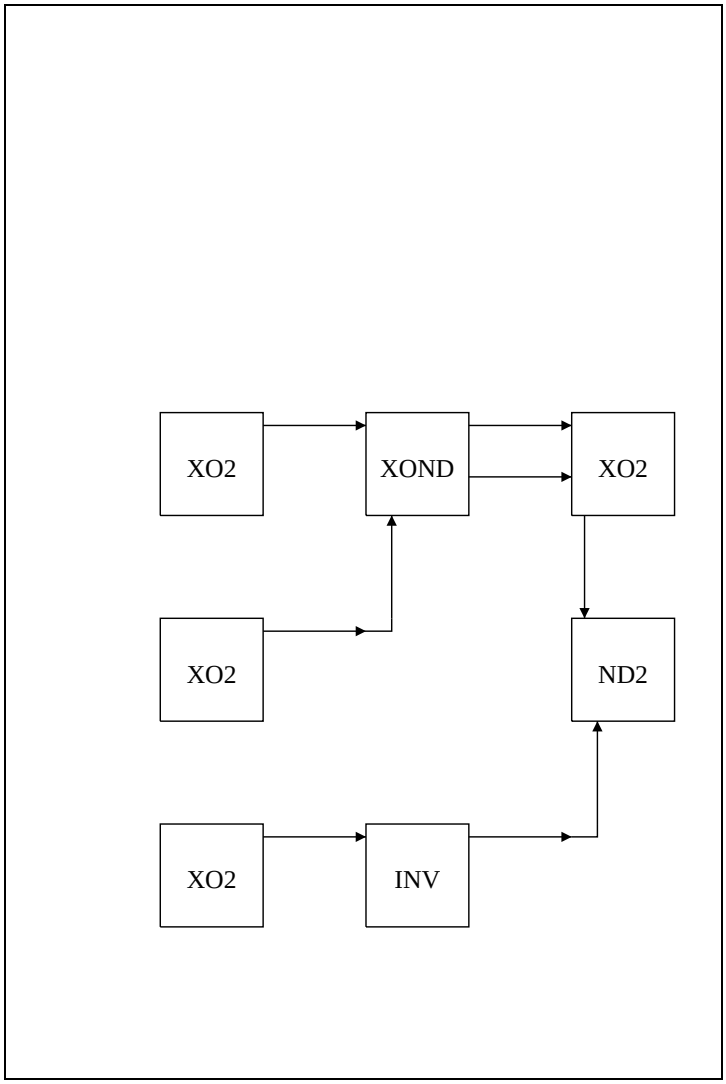
EC2 - 2-Bit Equality Comparator

Layout for Shape 1



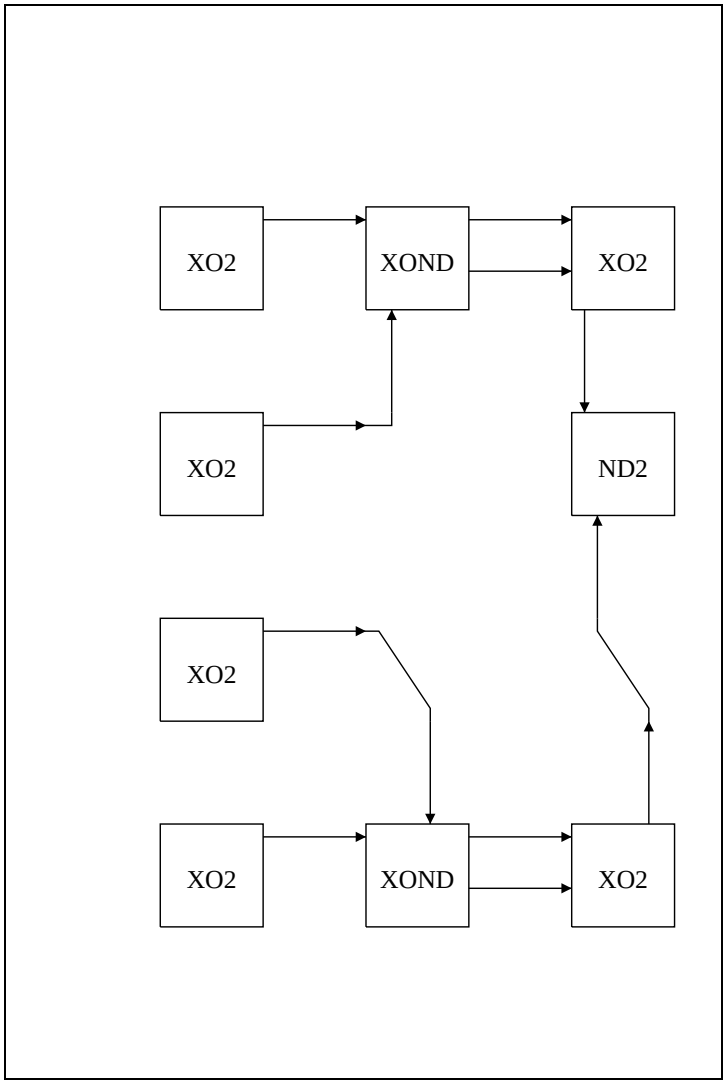
EC3 - 3-Bit Equality Comparator

Layout for Shape 1



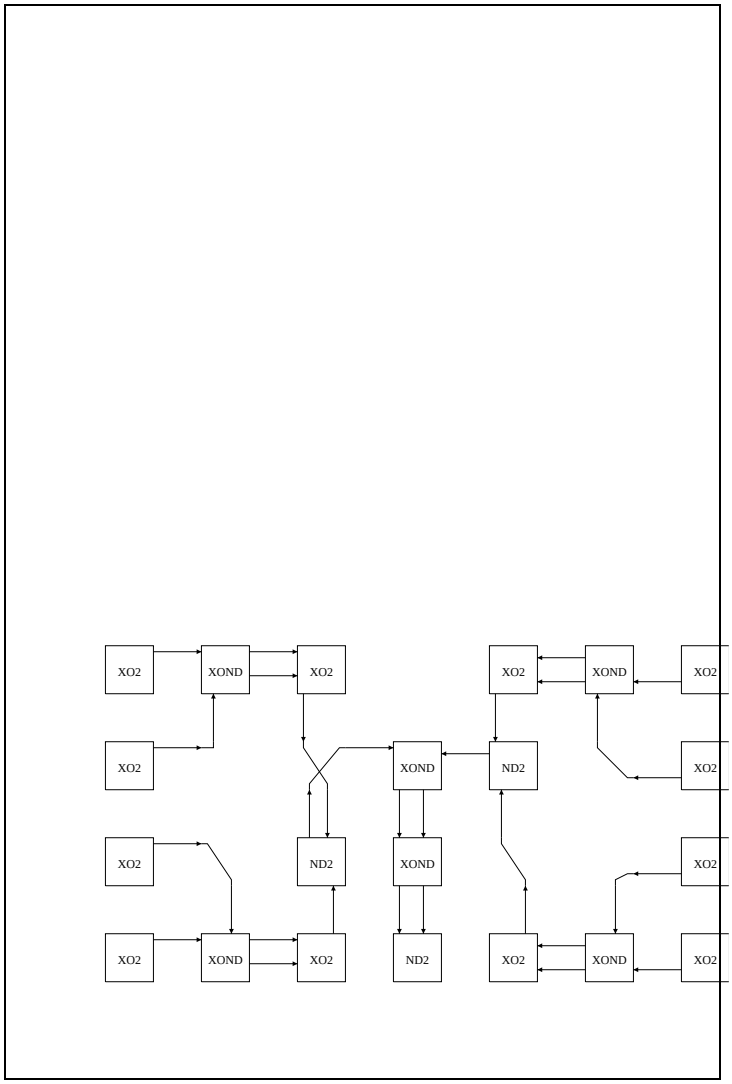
EC4 - 4-Bit Equality Comparator

Layout for Shape 1



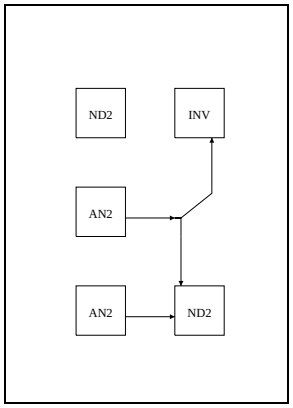
EC8 - 8-Bit Equality Comparator

Layout for Shape 1



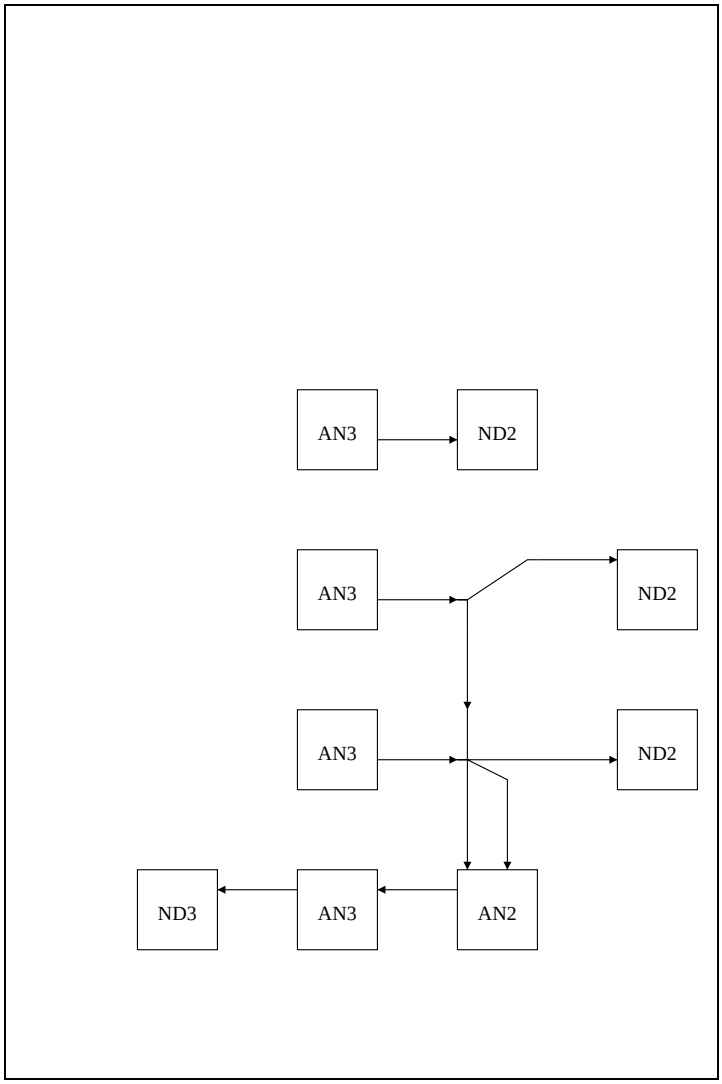
EN42 - 4-to-2 Encoder

Layout for Shape 1



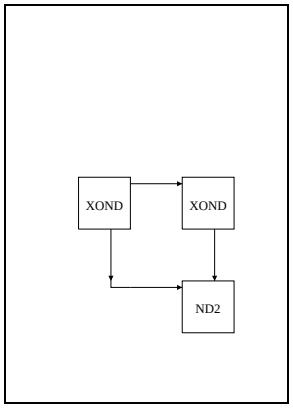
EN83 - 8-to-3 Encoder

Layout for Shape 1



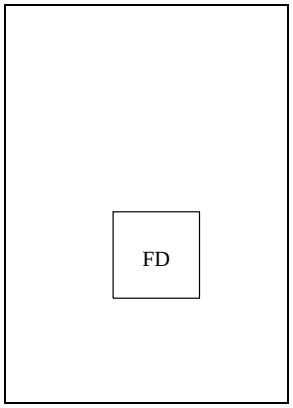
FA1 - 1-Bit Full Adder

Layout for Shape 1



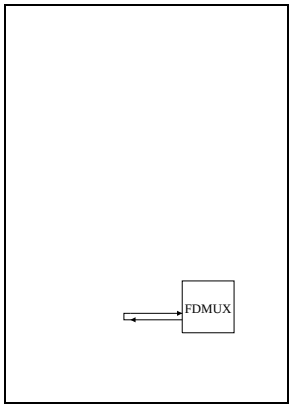
FD - D Flip-Flop Synchronous

Layout for Shape 1



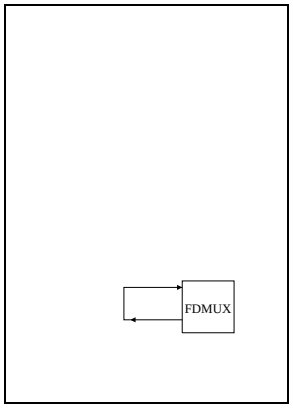
FDE - D Flip-Flop Synchronous with Enable

Layout for Shape 1



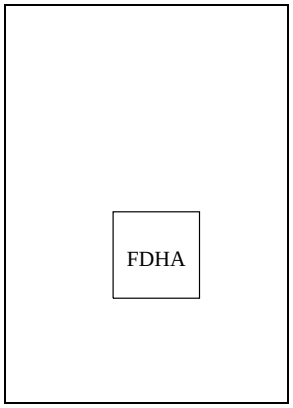
FDEL - D Flip-Flop Synch with Enable Low

Layout for Shape 1



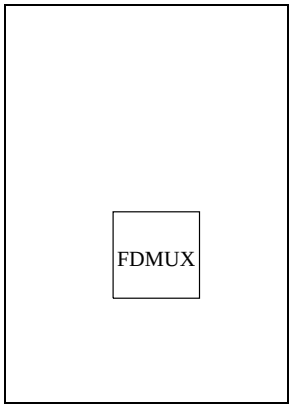
FDHA - D Flip-Flop Half-Adder Sum

Layout for Shape 1



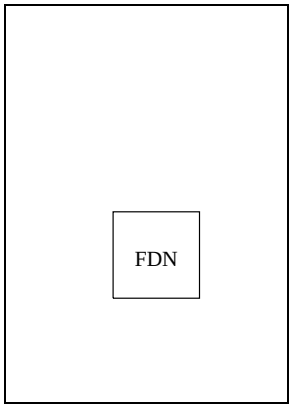
FDMUX - MUX Feeding D Flip-Flop

Layout for Shape 1



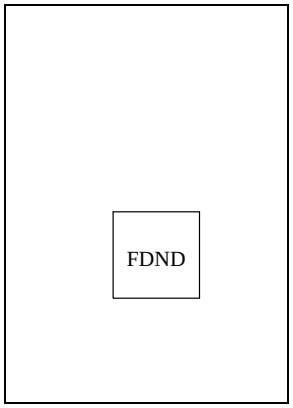
FDN - D Flip-Flop Synchronous with QN Out

Layout for Shape 1



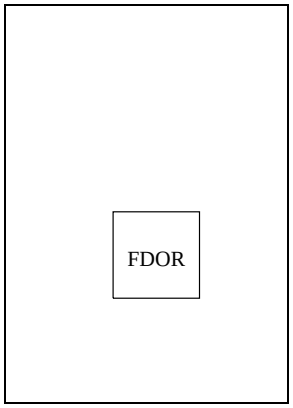
FDND - D Flip-Flop 2 Input NAND

Layout for Shape 1



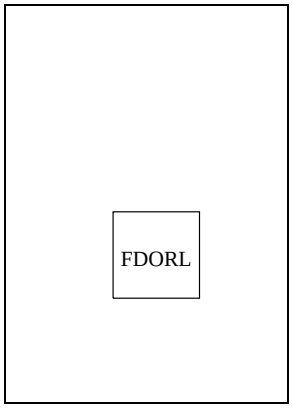
FDOR - D Flip-Flop 2 Input OR

Layout for Shape 1



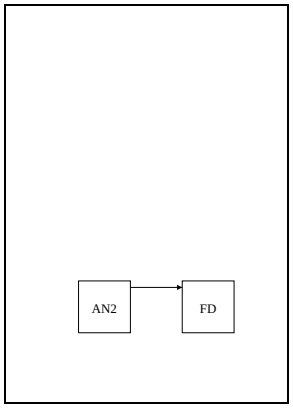
FDORL - D Flip-Flop (A+L')

Layout for Shape 1



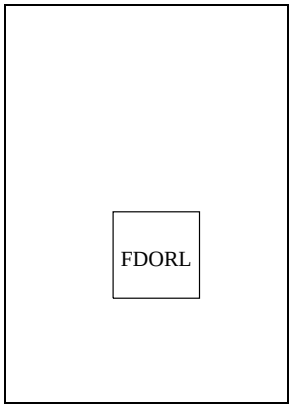
FDR - D Flip-Flop Synchronous Reset Low

Layout for Shape 1



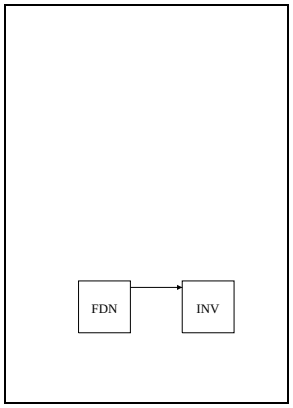
FDS - D Flip-Flop Synchronous Set Low

Layout for Shape 1



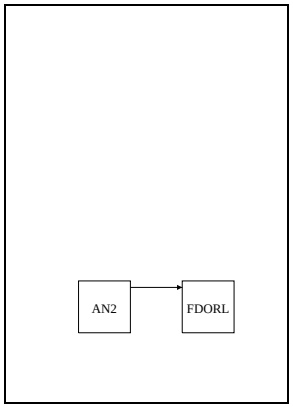
FDSA - D Flip-Flop Asynchronous Set Low

Layout for Shape 1



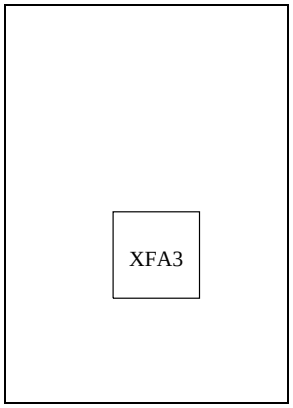
FDSR - D Flip-Flop Sync Set/Reset Low

Layout for Shape 1



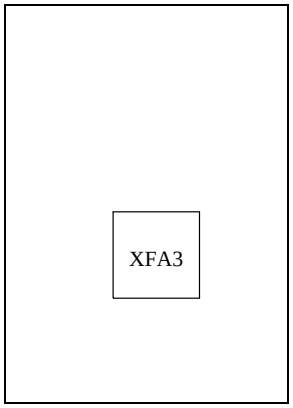
FDXO - D Flip-Flop with XOR

Layout for Shape 1



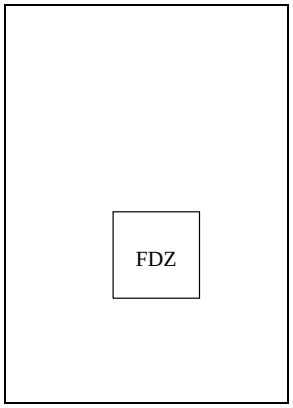
FDXOAN3 - (A*L) XOR B; B = (A*L) AND B

Layout for Shape 1



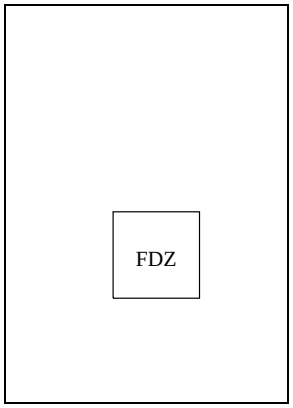
FDZ - D Flip-Flop with Tristate Out

Layout for Shape 1



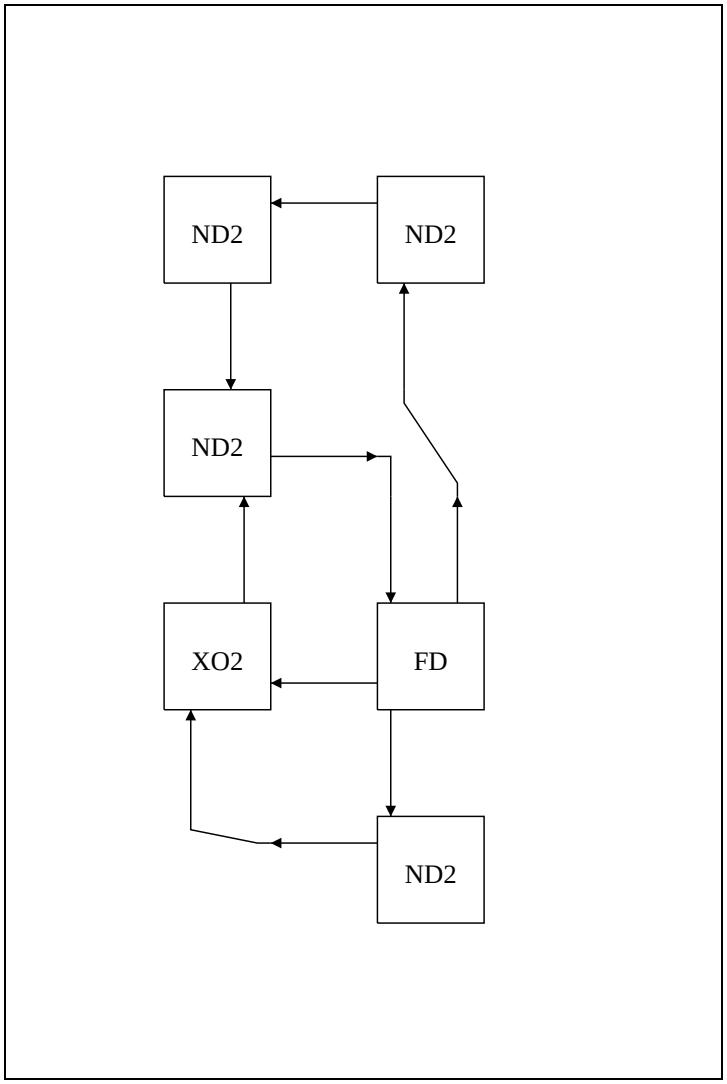
FDZQ - D Flip-Flop with Tristate Out and Q Out

Layout for Shape 1



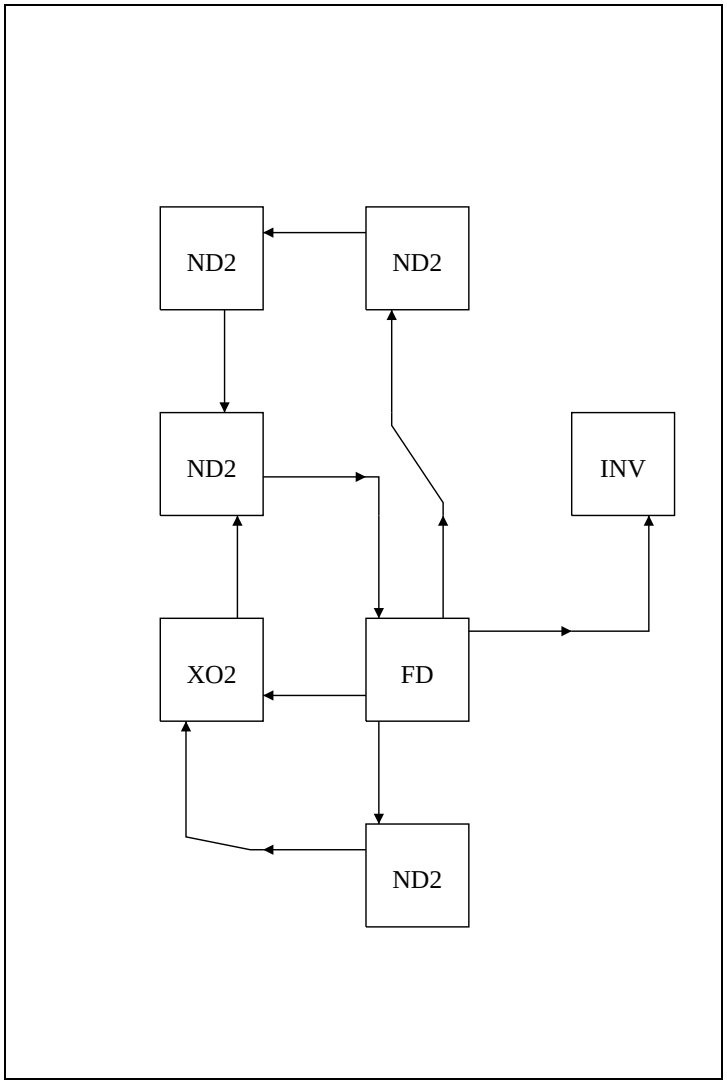
FJK - JK Flip-Flop Synchronous

Layout for Shape 1



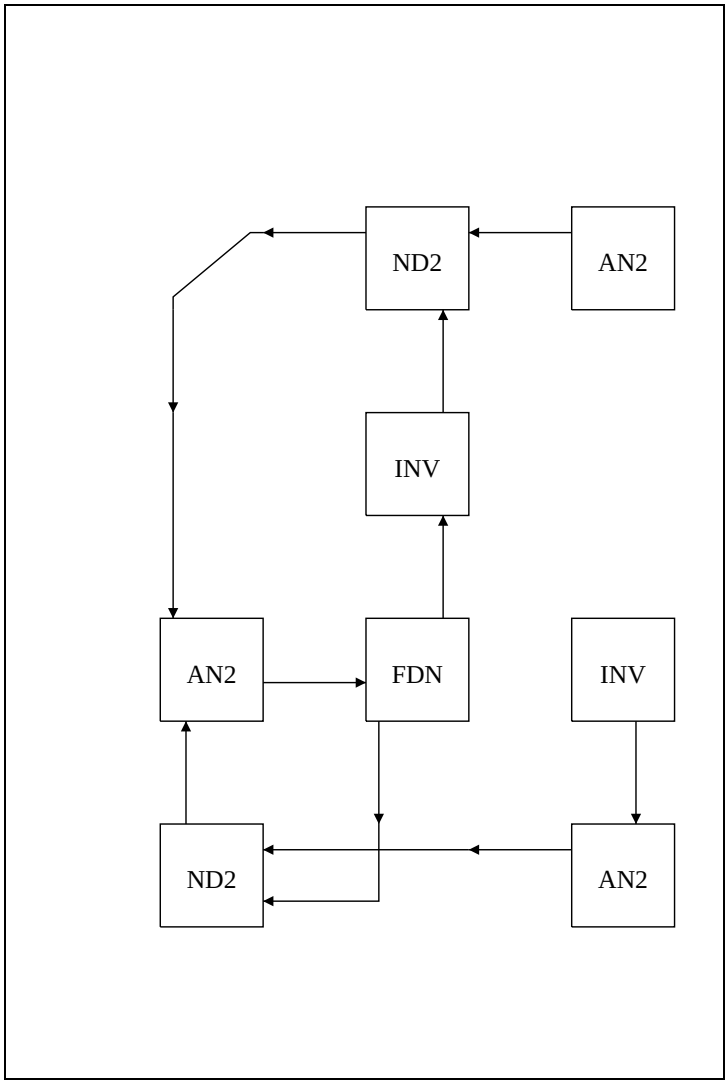
FJKQ - JK Flip-Flop Synchronous with Q Low

Layout for Shape 1



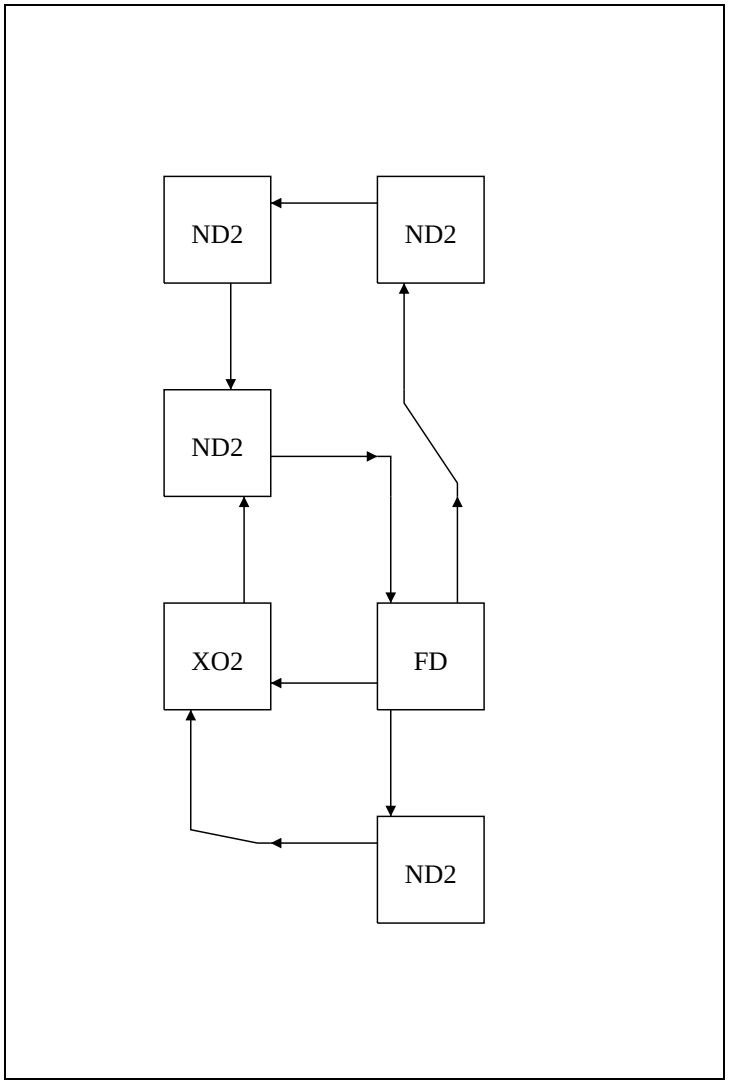
FJKR - JK Flip-Flop Synchronous Reset Low

Layout for Shape 1



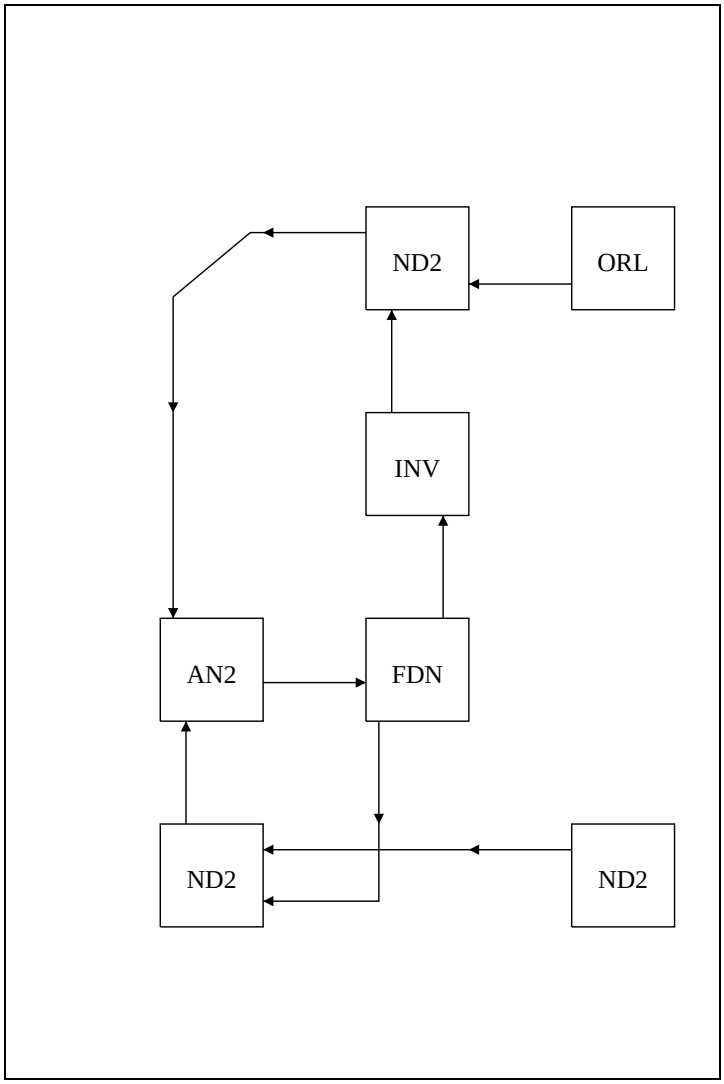
FJKRA - JK Flip-Flop Asynchronous Reset Low

Layout for Shape 1



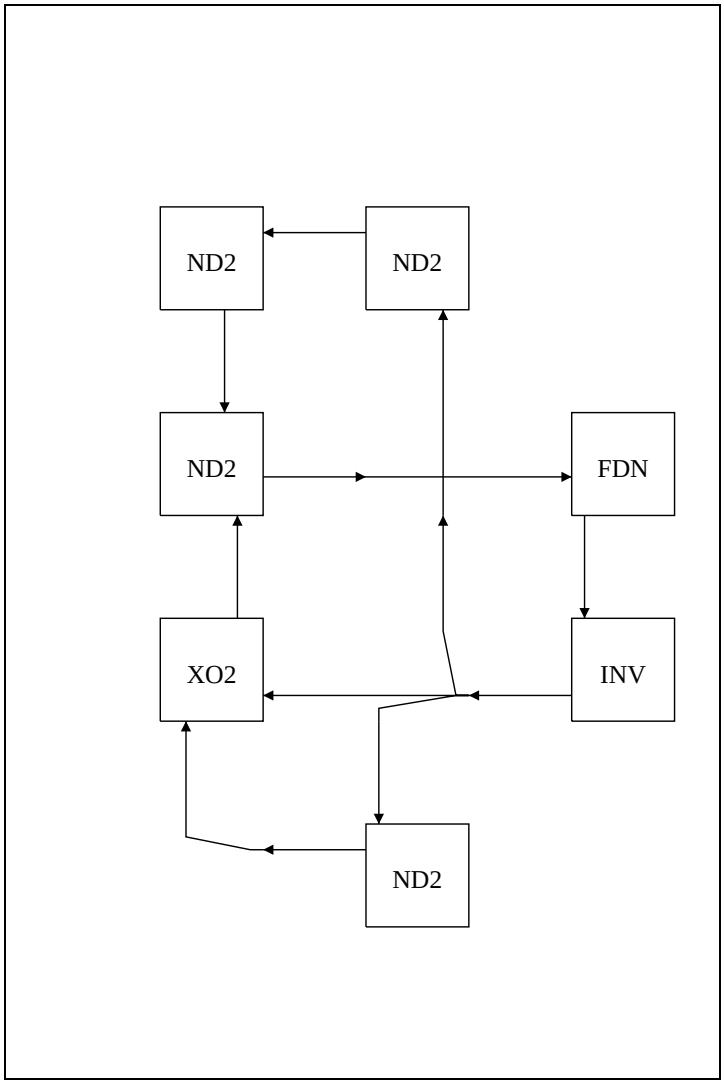
FJKS - JK Flip-Flop Synchronous Set Low

Layout for Shape 1



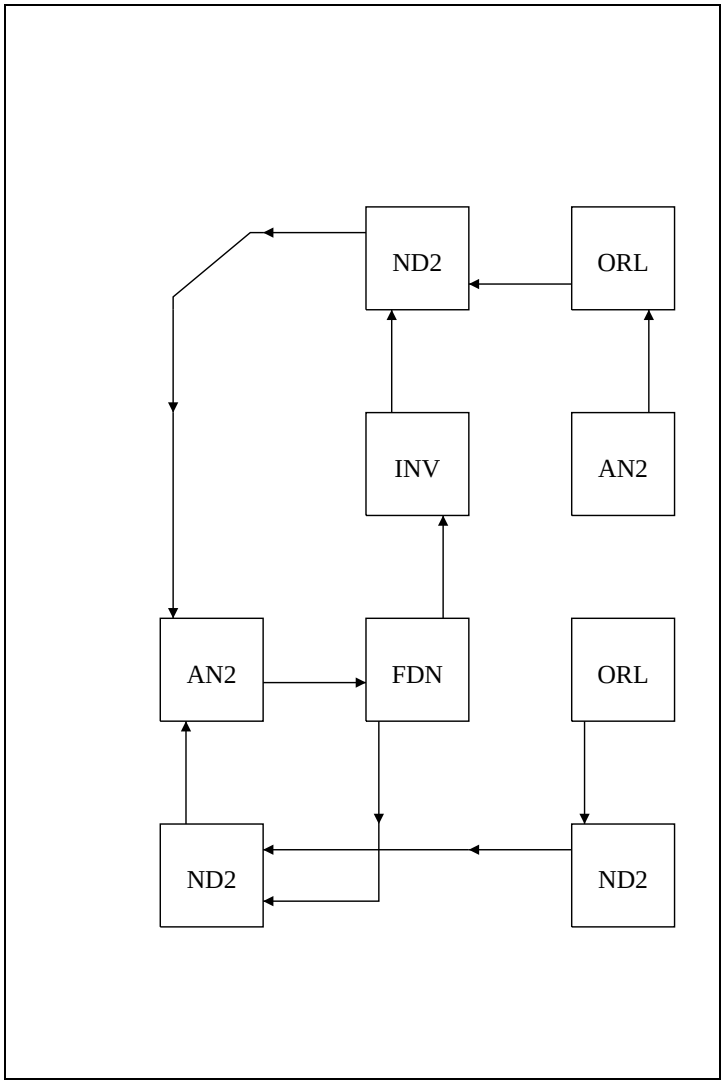
FJKSA - JK Flip-Flop Asynchronous Set Low

Layout for Shape 1



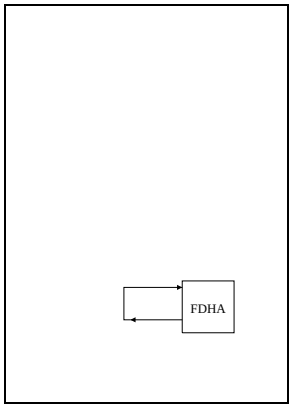
FJKSR - JK Flip-Flop Synch Set/Reset Low

Layout for Shape 1



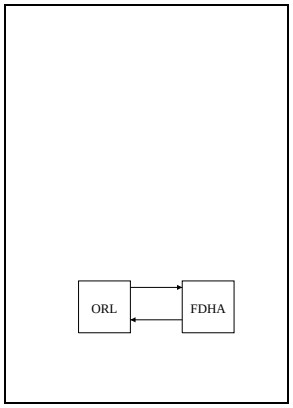
FT - T Flip-Flop Synchronous

Layout for Shape 1



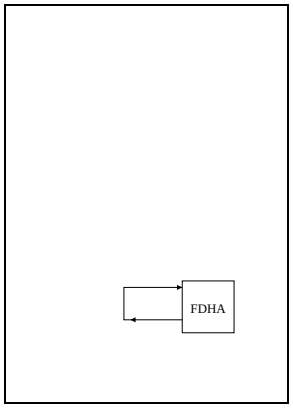
FTR - T Flip-Flop Synchronous Reset Low

Layout for Shape 1



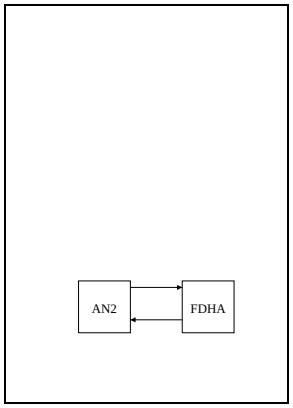
FTRA - T Flip-Flop Asynchronous Reset Low

Layout for Shape 1



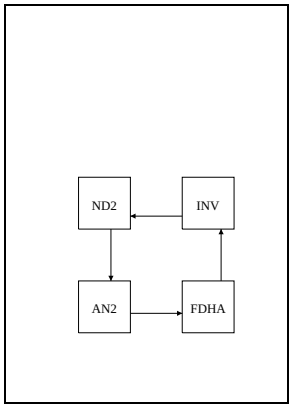
FTS - T Flip-Flop Synchronous Set Low

Layout for Shape 1



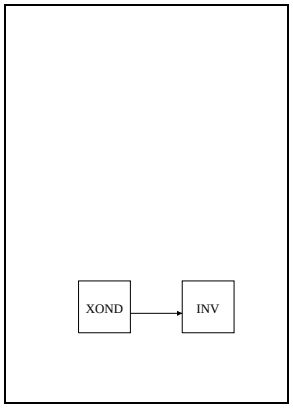
FTSR - T Flip-Flop Synchronous Set/Reset Low

Layout for Shape 1



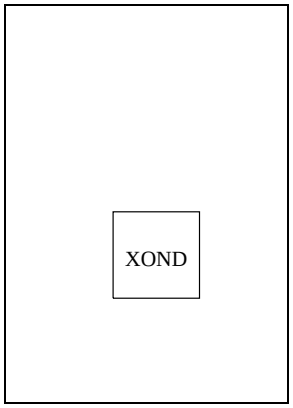
HA1 - 1-Bit Half Adder

Layout for Shape 1



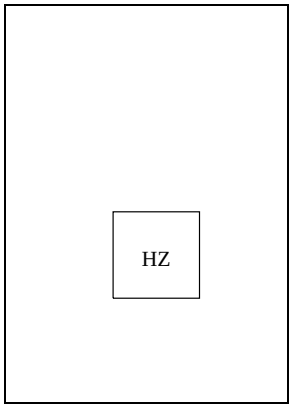
HAL1 - 1-Bit Half Adder Carry Low

Layout for Shape 1



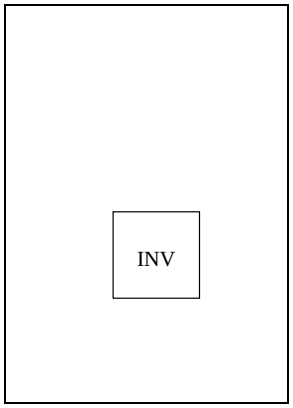
HZ - Bus Driver High or Z

Layout for Shape 1



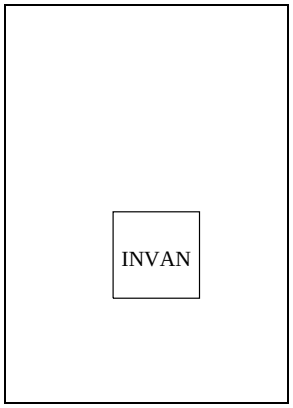
INV - Inverter

Layout for Shape 1



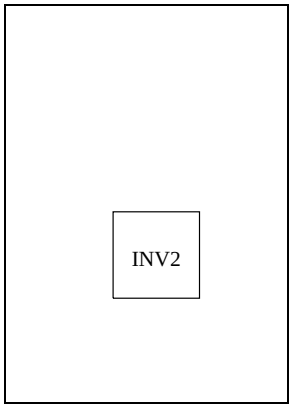
INVAN2 - Inverter and 2-Input AND L', (A*L)

Layout for Shape 1



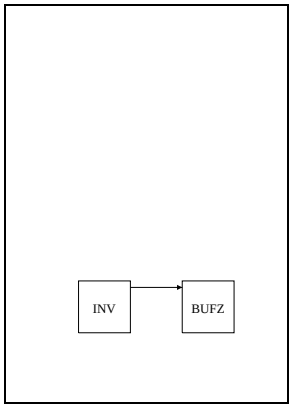
INVINV - Twin Inverters

Layout for Shape 1



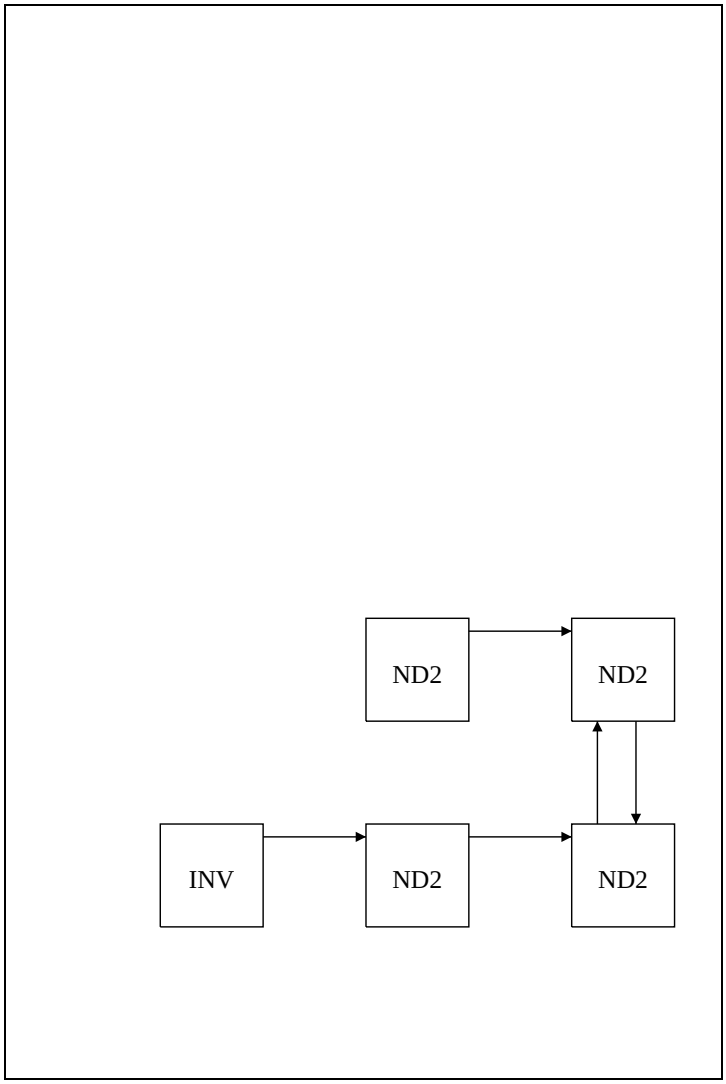
INVZ - Tristate Inverter

Layout for Shape 1



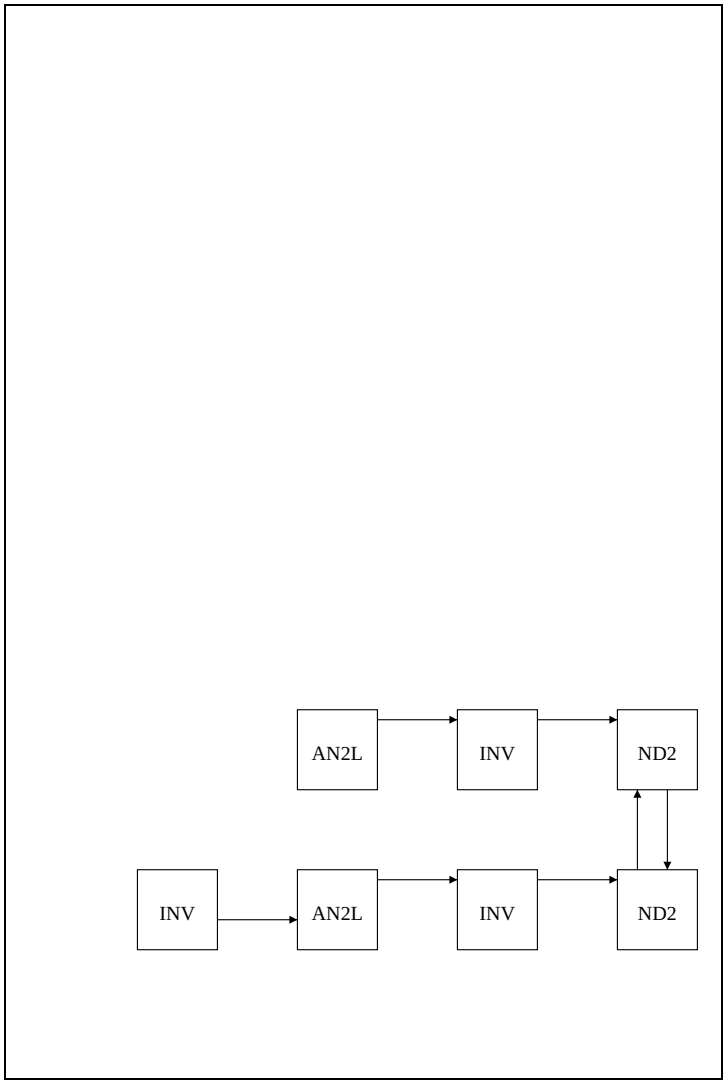
LD - D Latch Transparent High

Layout for Shape 1



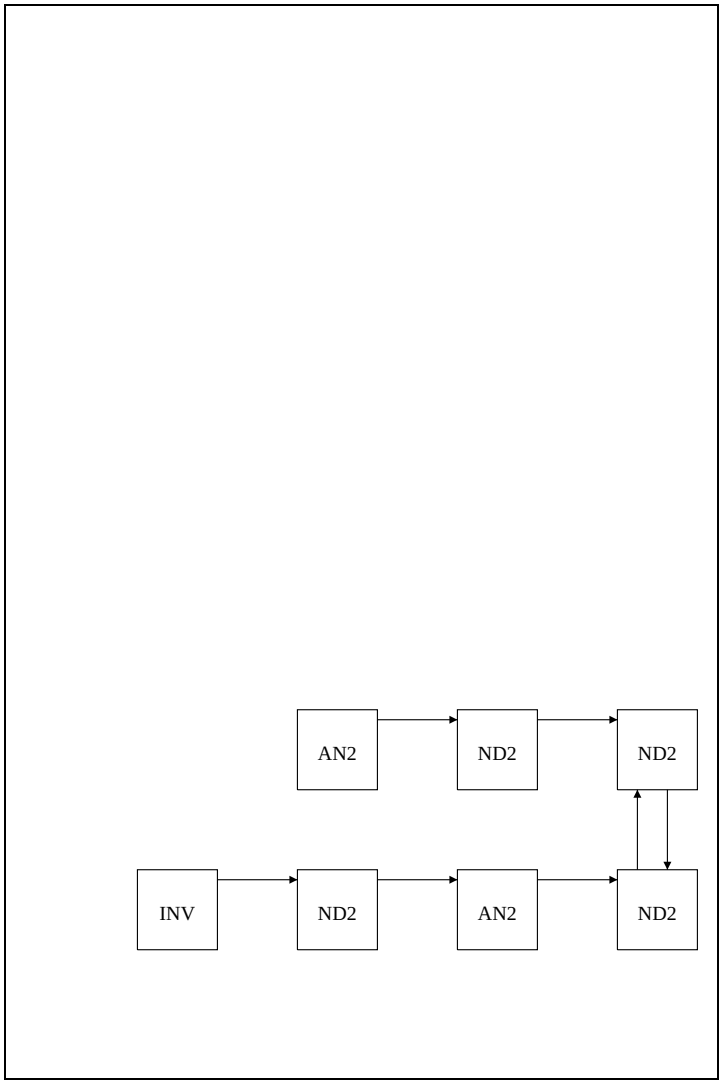
LDL - D Latch Transparent Low

Layout for Shape 1



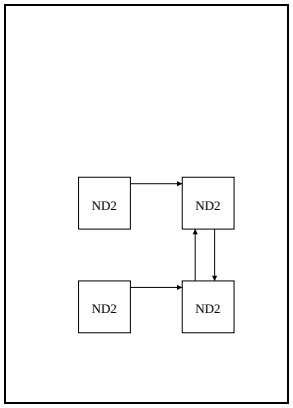
LDR - D Latch Transparent High, Reset Low

Layout for Shape 1



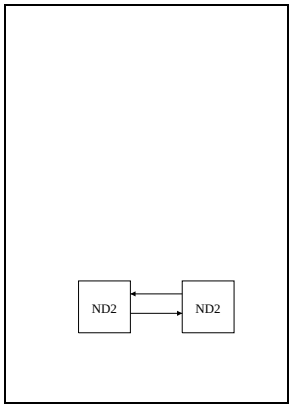
LSREN - SR Latch with NAND with Enable

Layout for Shape 1



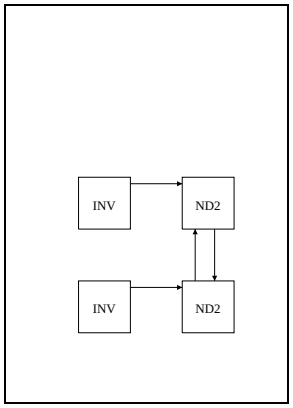
LSRND - SR Latch with NAND

Layout for Shape 1



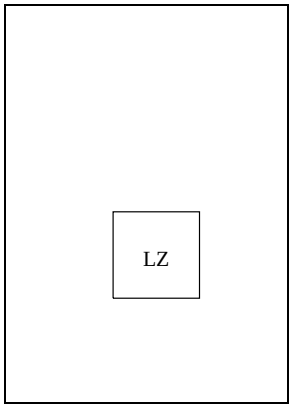
LSRNR - SR Latch with NOR

Layout for Shape 1



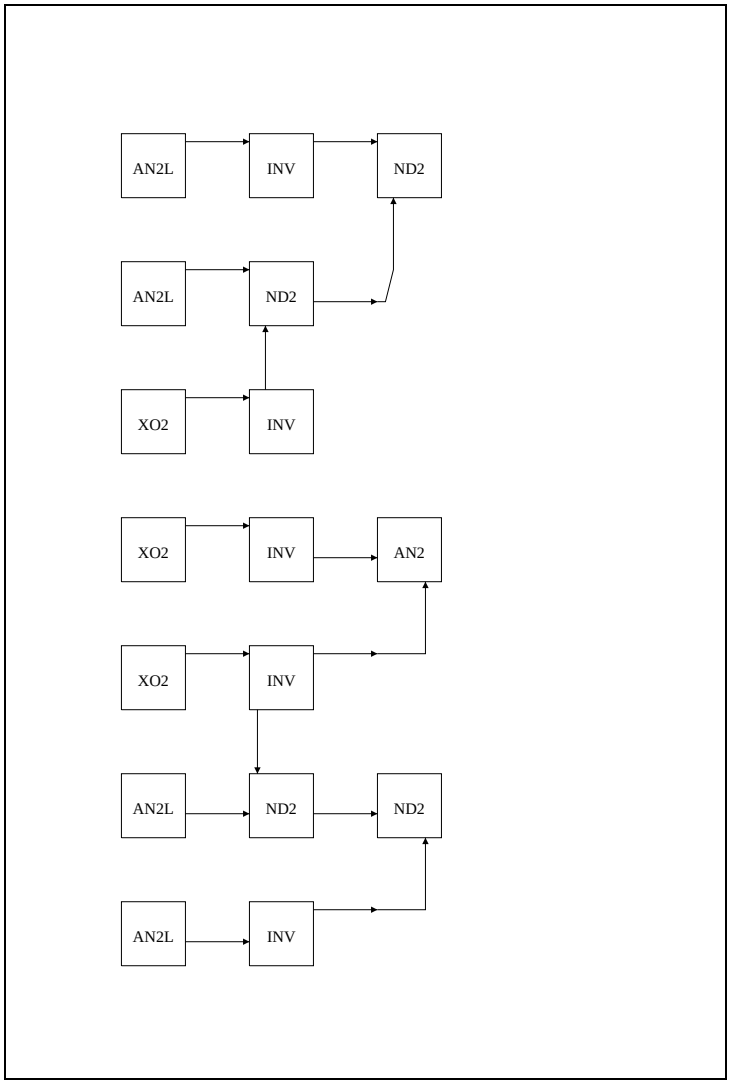
LZ - Bus Driver Low or Z

Layout for Shape 1



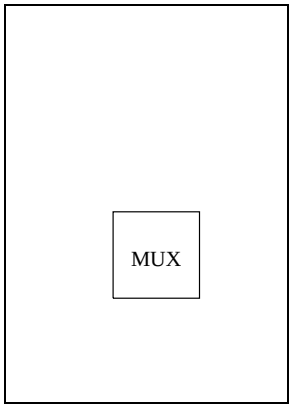
MC2 - 2-Bit Magnitude Comparator

Layout for Shape 1



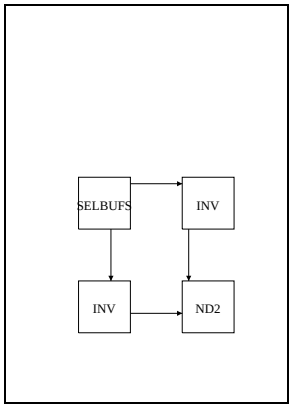
MUX - 2-to-1 Multiplexer(FAST)(A*B')XOR(A*B)

Layout for Shape 1



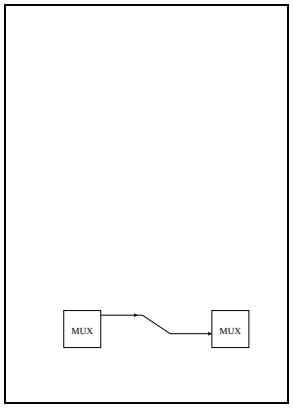
MUX21 - 2-to-1 Multiplexer

Layout for Shape 1



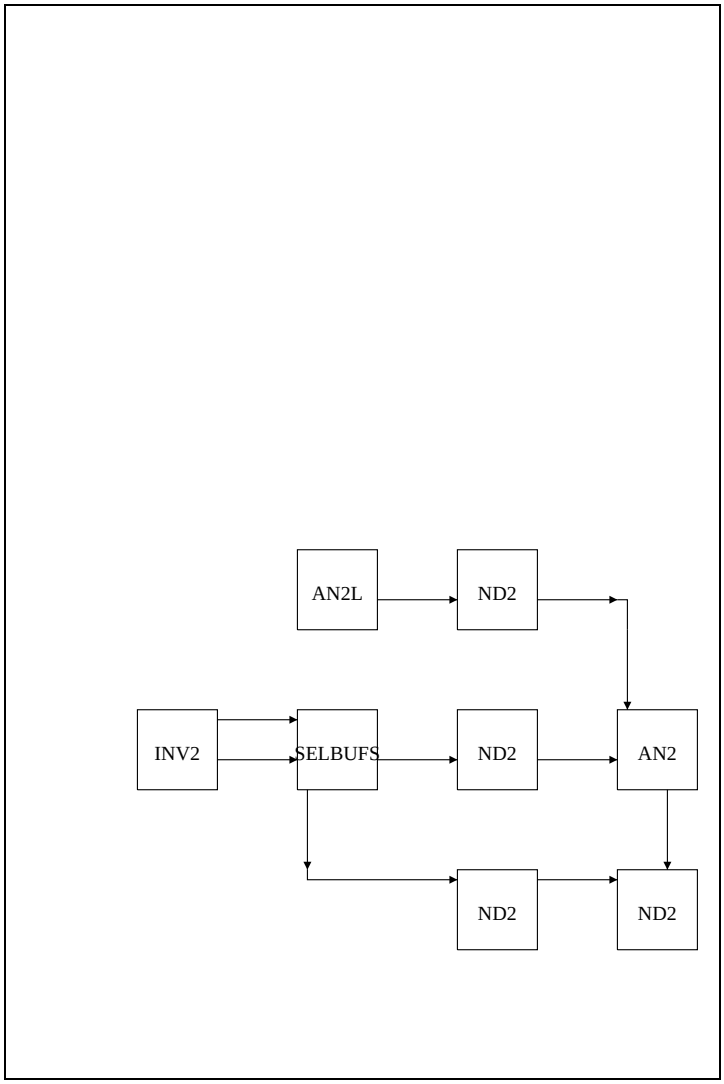
MUX3 - 3-to-1 Multiplexer (Fast)

Layout for Shape 1



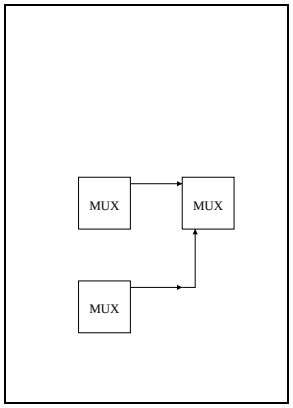
MUX31 - 3-to-1 Multiplexer

Layout for Shape 1



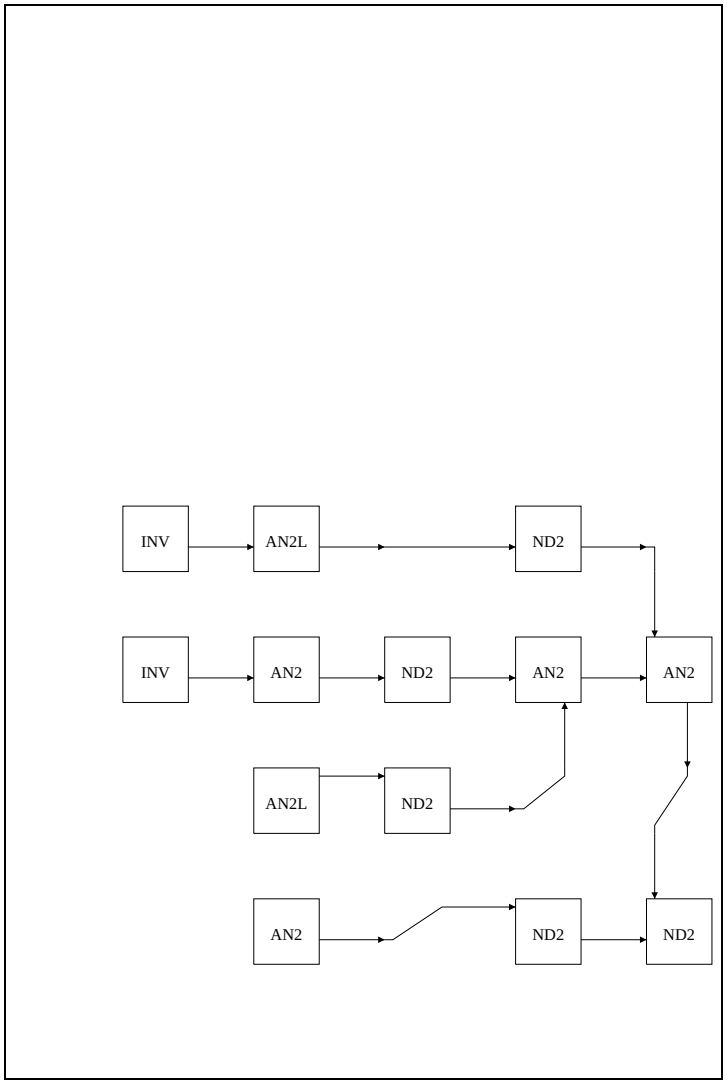
MUX4 - 4-to-1 Multiplexer (Fast)

Layout for Shape 1



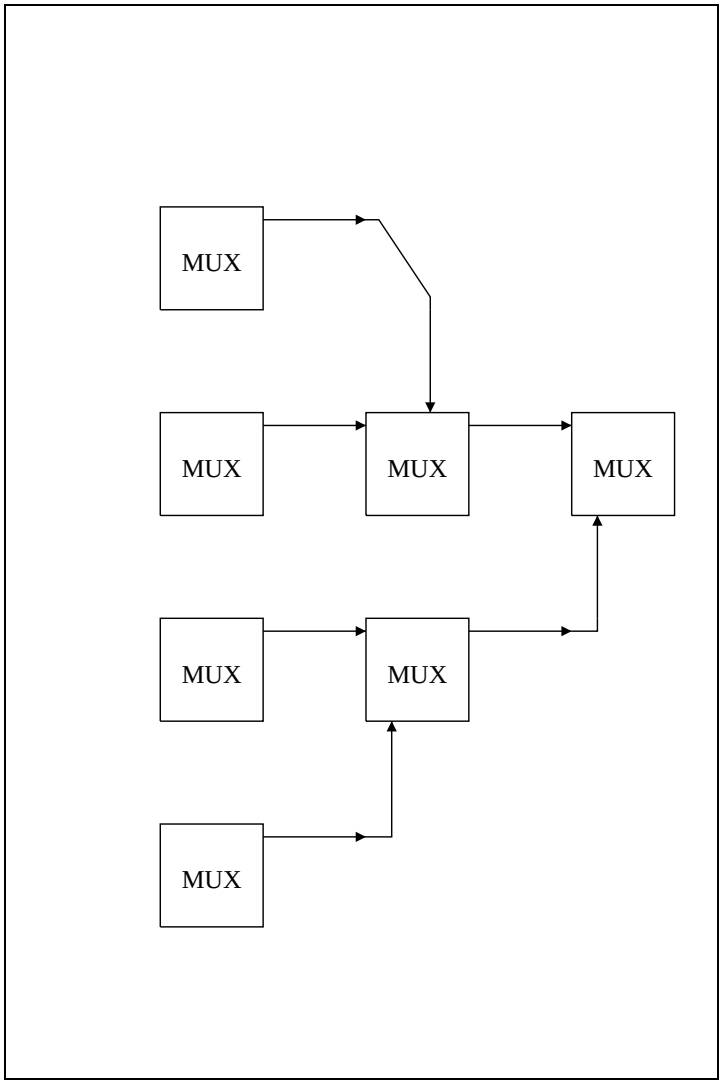
MUX41 - 4-to-1 Multiplexer

Layout for Shape 1



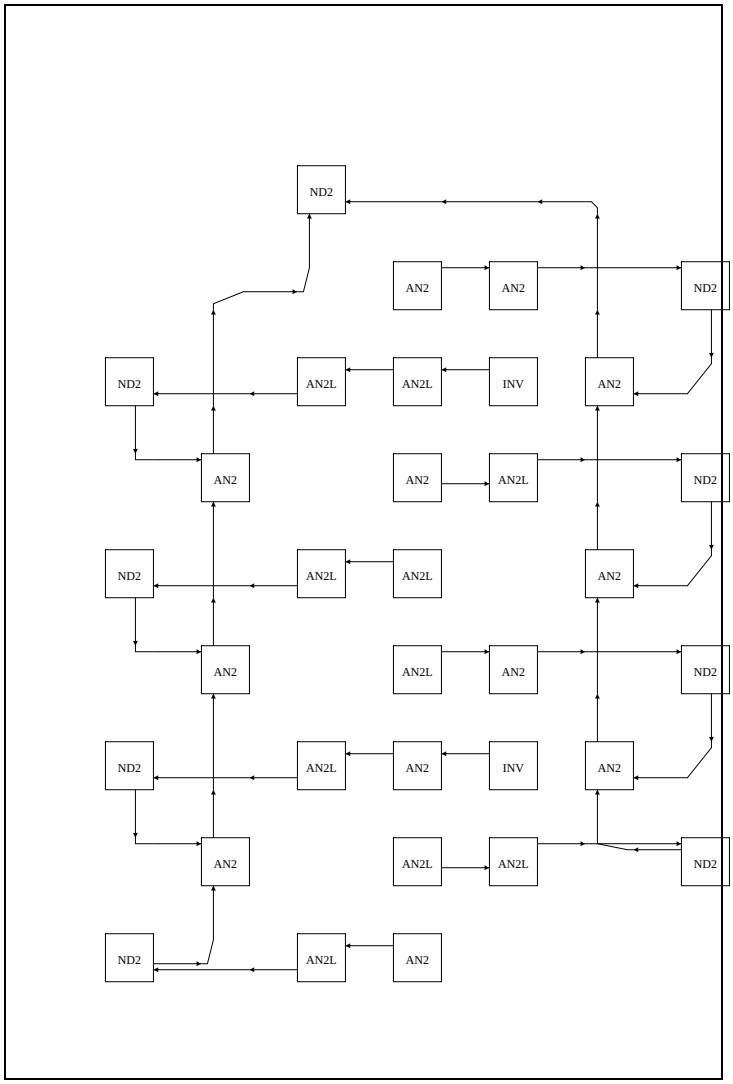
MUX8 - 8-to-1 Multiplexer (Fast)

Layout for Shape 1



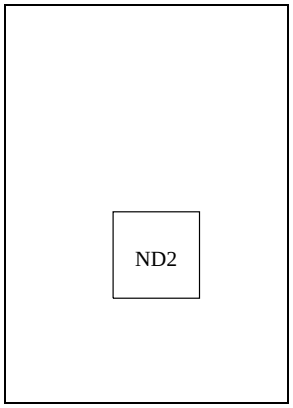
MUX81 - 8-to-1 Multiplexer

Layout for Shape 1



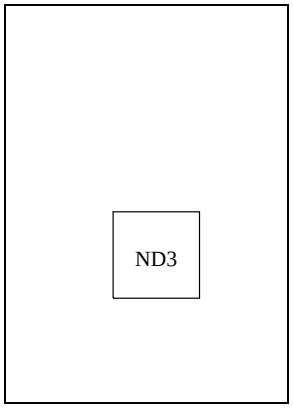
ND2 - 2-Input NAND

Layout for Shape 1



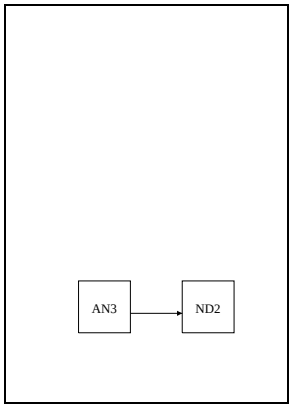
ND3 - 3-Input NAND

Layout for Shape 1



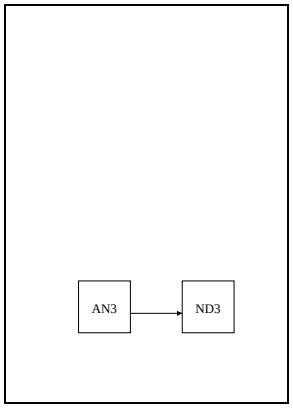
ND4 - 4-Input NAND

Layout for Shape 1



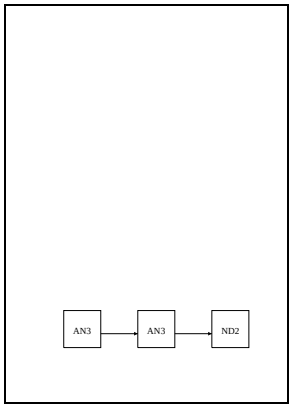
ND5 - 5-Input NAND

Layout for Shape 1



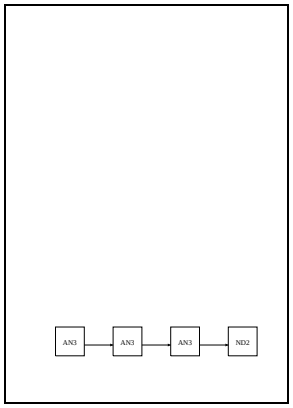
ND6 - 6-Input NAND

Layout for Shape 1



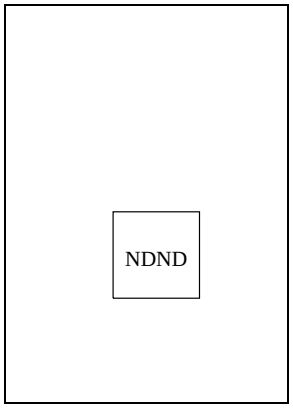
ND8 - 8-Input NAND

Layout for Shape 1



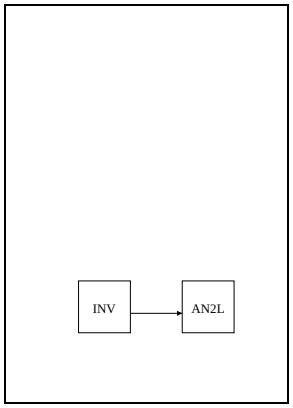
NDND - Twin 2-Input NANDs

Layout for Shape 1



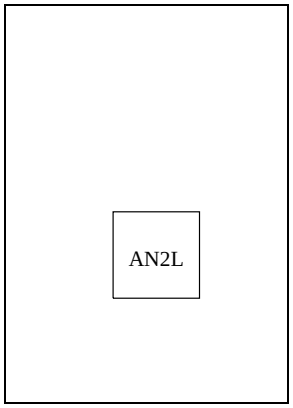
NR2 - 2-Input NOR

Layout for Shape 1



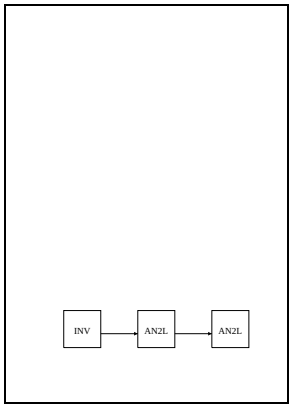
NR2L - 2-Input NOR with Inverted Input (A*B')

Layout for Shape 1



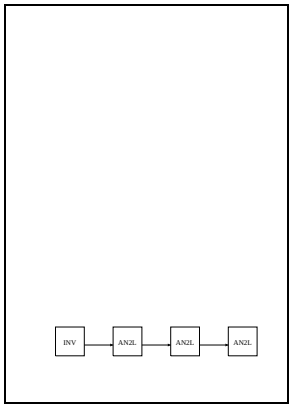
NR3 - 3-Input NOR

Layout for Shape 1



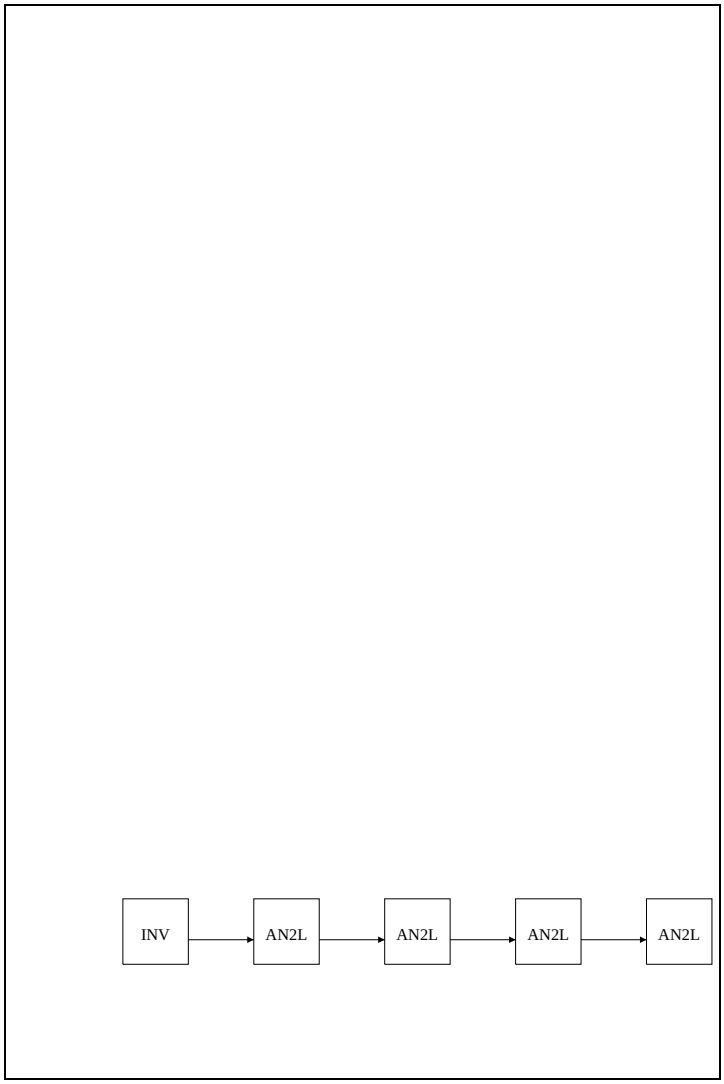
NR4 - 4-Input NOR

Layout for Shape 1



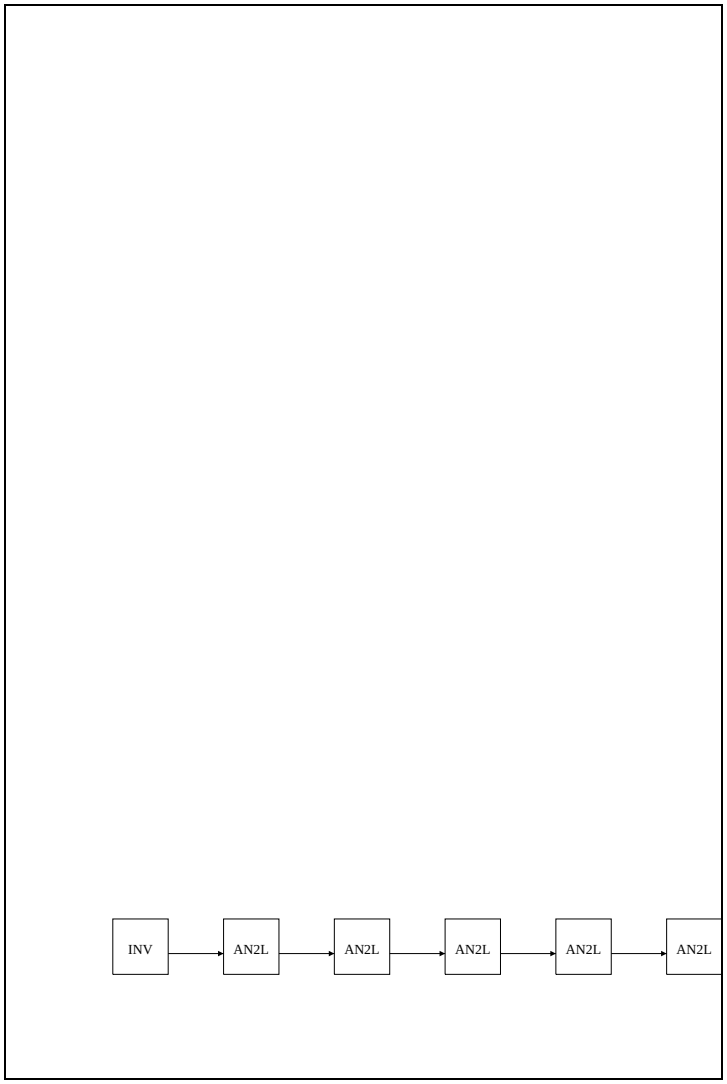
NR5 - 5-Input NOR

Layout for Shape 1



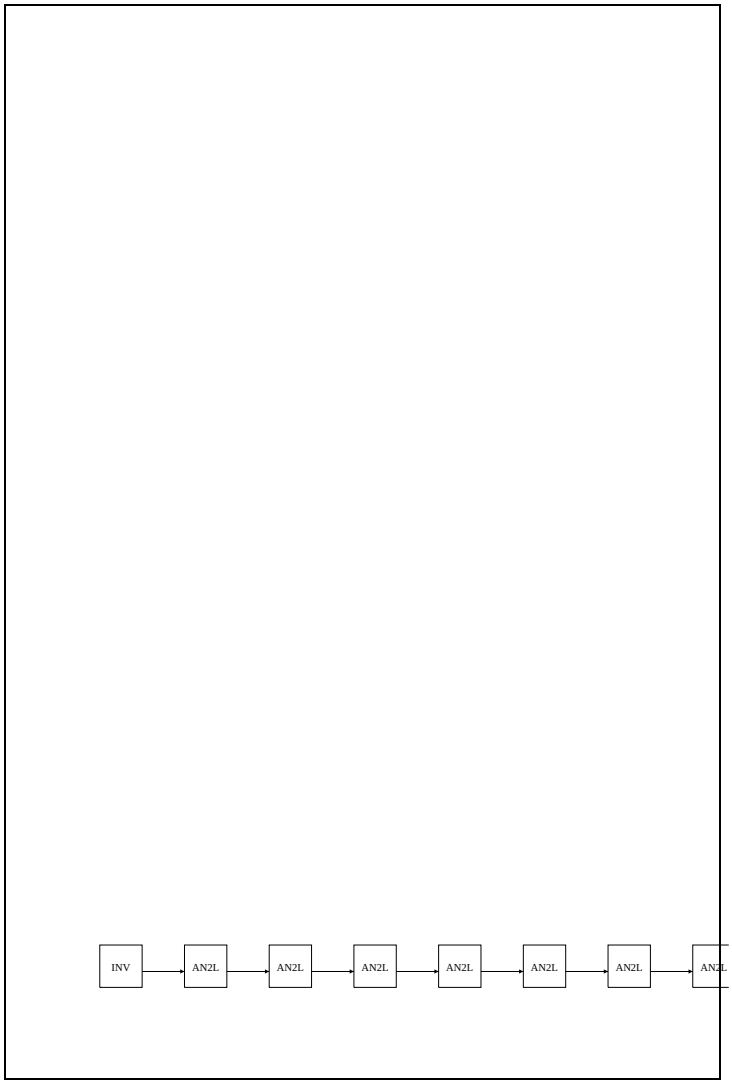
NR6 - 6-Input NOR

Layout for Shape 1



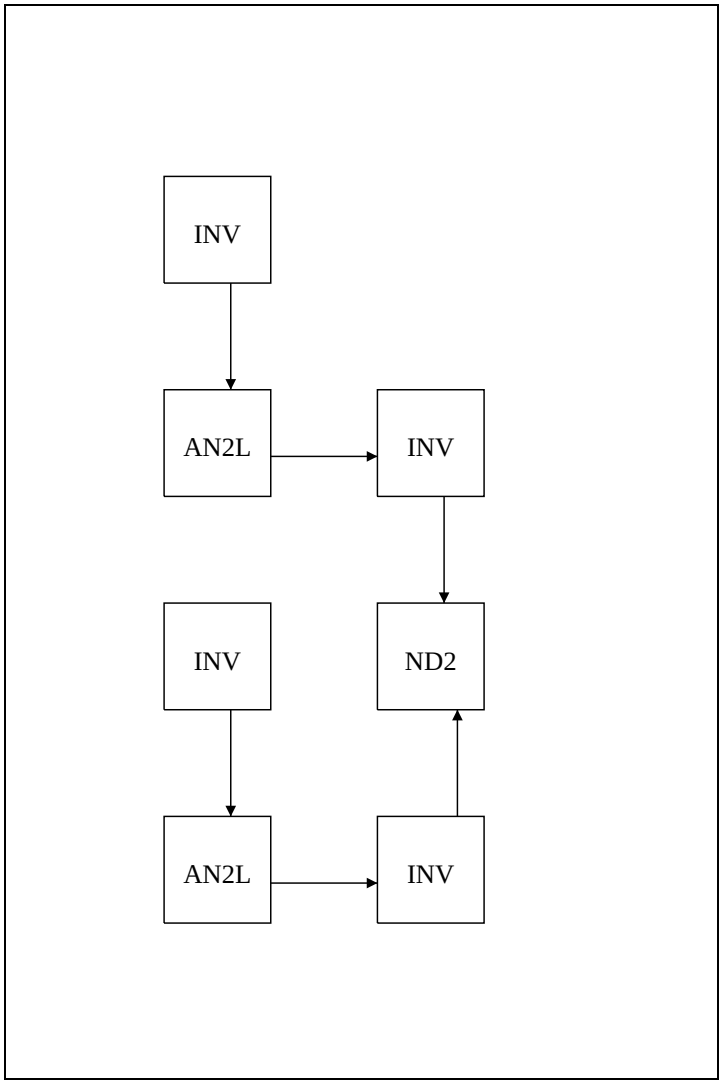
NR8 - 8-Input NOR

Layout for Shape 1



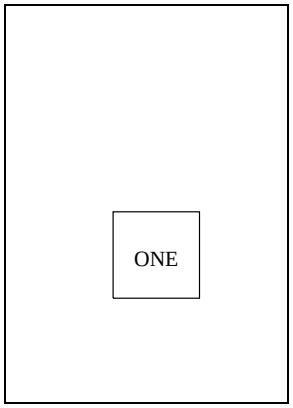
OAI22 - OR-AND Inverter 2-2 Inputs

Layout for Shape 1



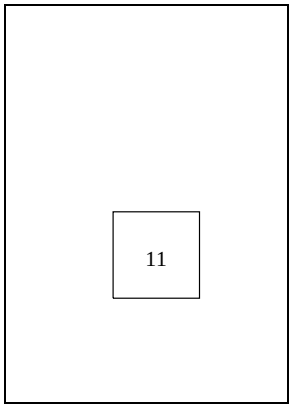
ONE/ONEB - Logic One

Layout for Shape 1



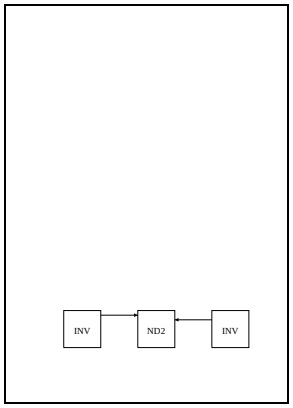
ONEONE - Twin Logic Ones

Layout for Shape 1



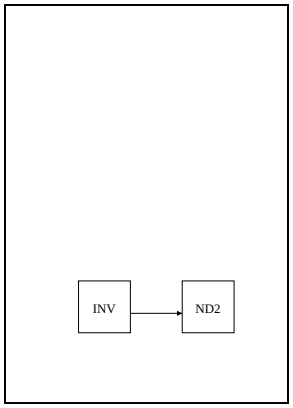
OR2 - 2-Input OR

Layout for Shape 1



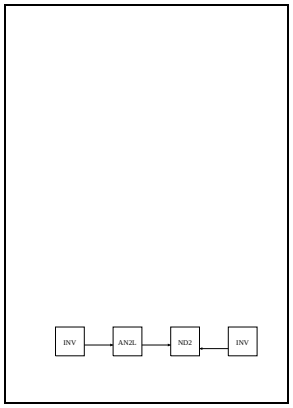
OR2L - 2-Input OR (A+B')

Layout for Shape 1



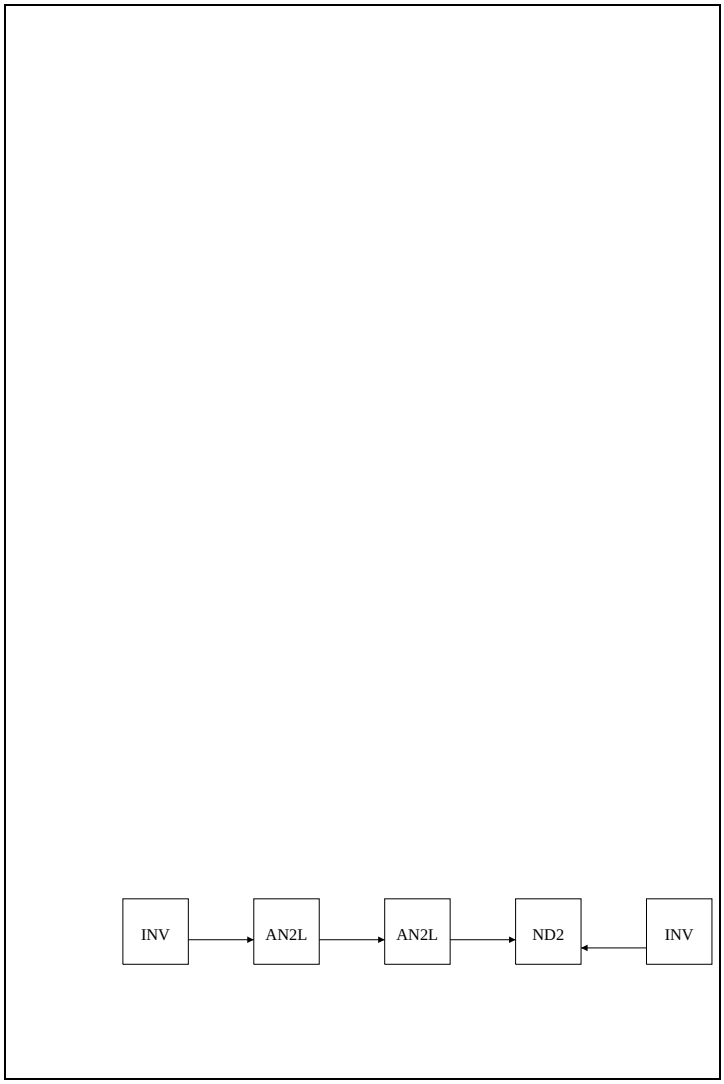
OR3 - 3-Input OR

Layout for Shape 1



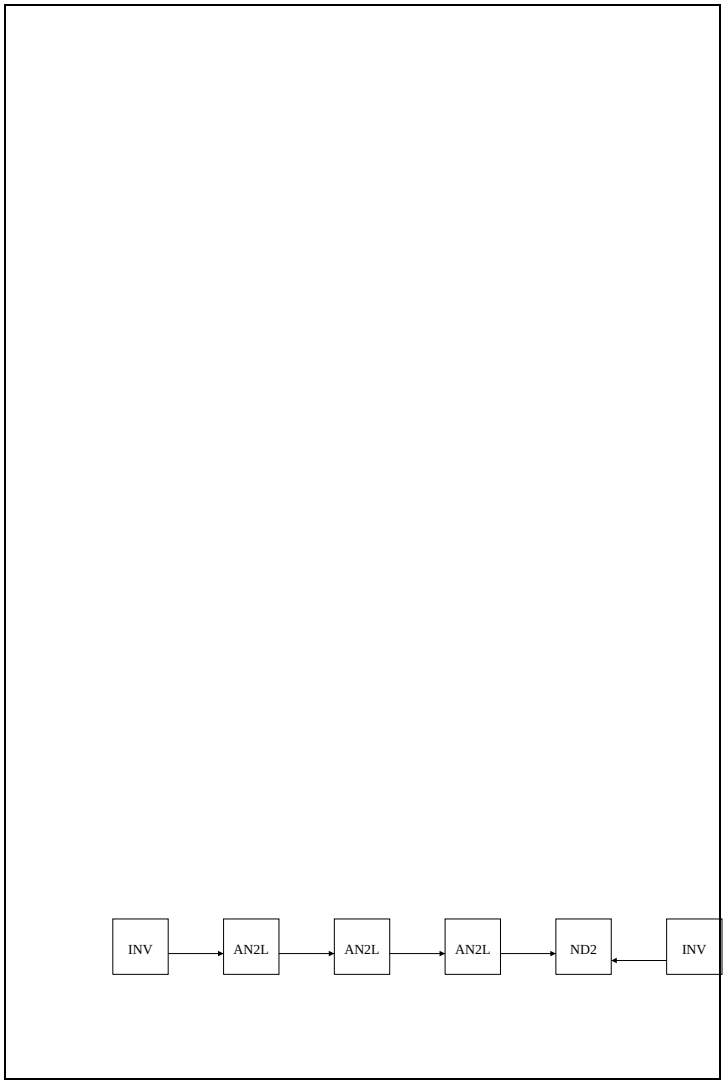
OR4 - 4-Input OR

Layout for Shape 1



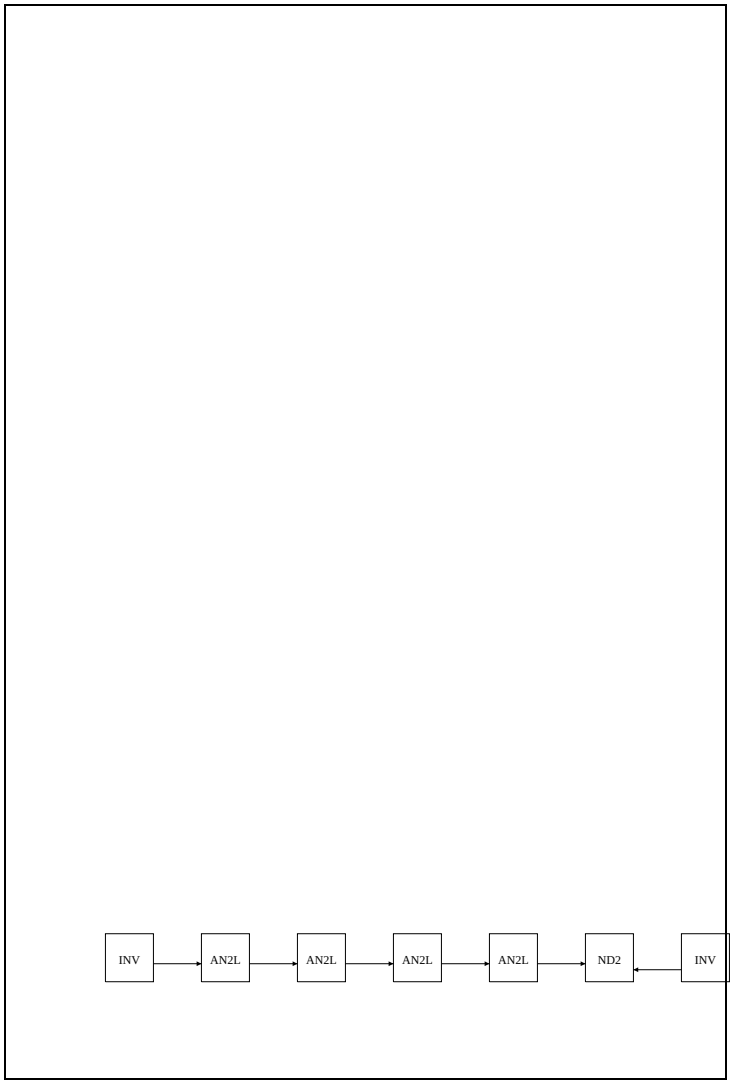
OR5 - 5-Input OR

Layout for Shape 1



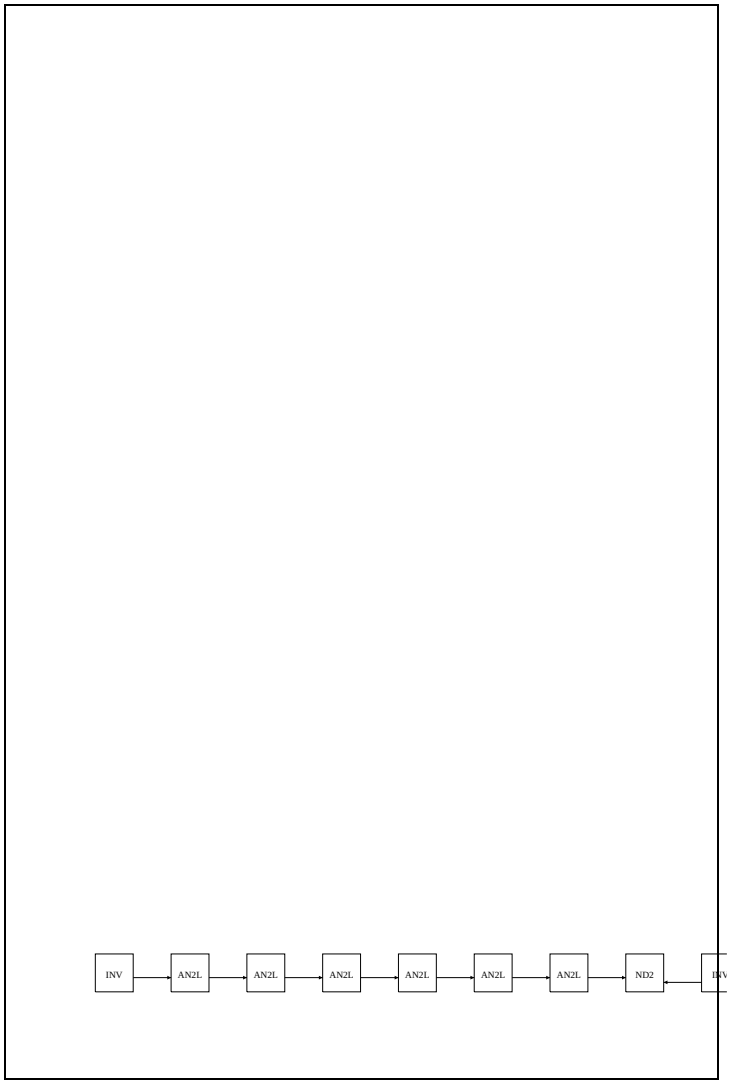
OR6 - 6-Input OR

Layout for Shape 1



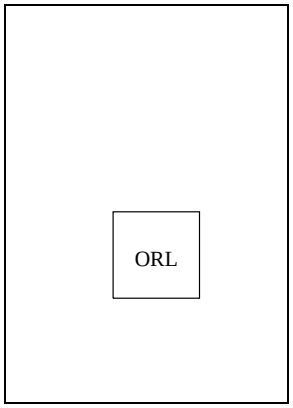
OR8 - 8-Input OR

Layout for Shape 1



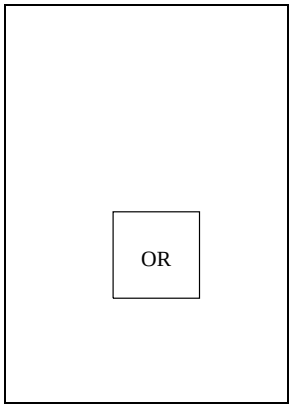
ORL - 2-Input OR (AN*B) XOR AN'

Layout for Shape 1



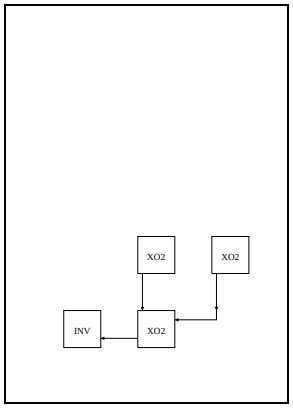
ORT - 2-Input OR = (A*B') XOR B

Layout for Shape 1



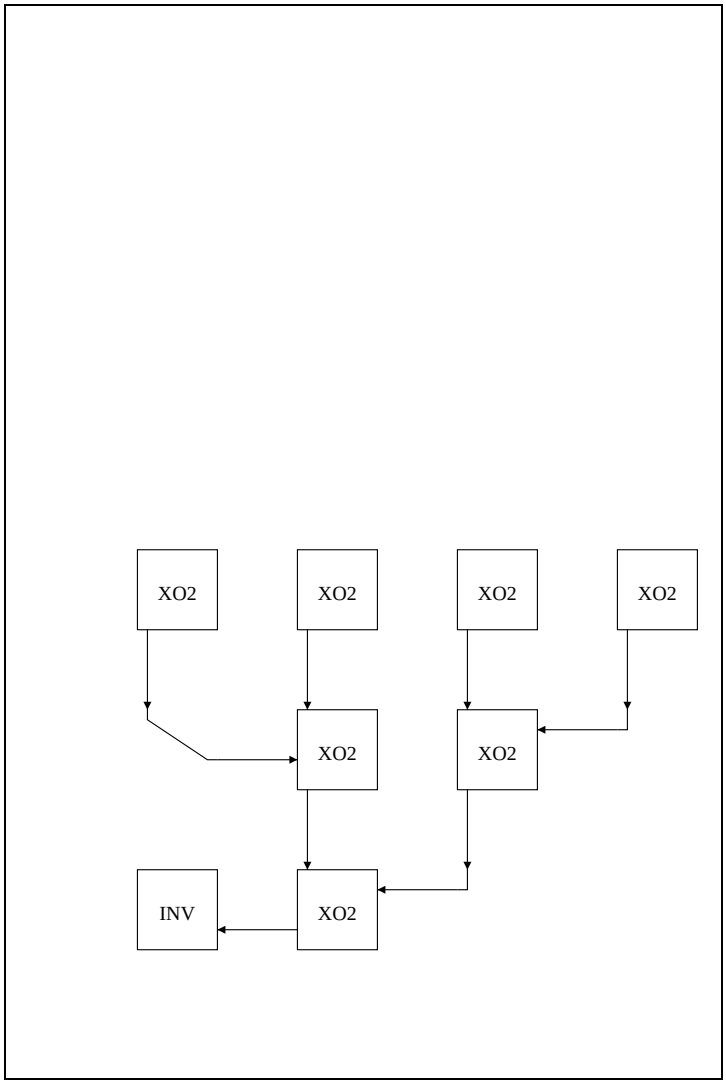
PCOE4 - 4-Bit Parity Checker Odd/Even

Layout for Shape 1



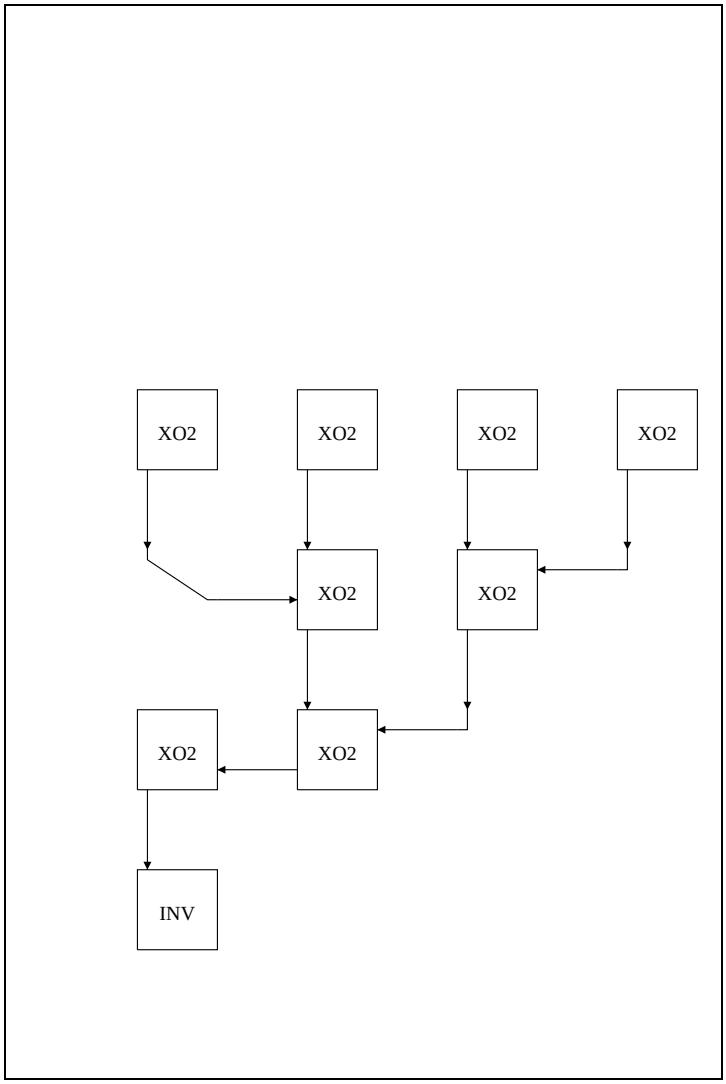
PCOE8 - 8-Bit Parity Checker Odd/Even

Layout for Shape 1



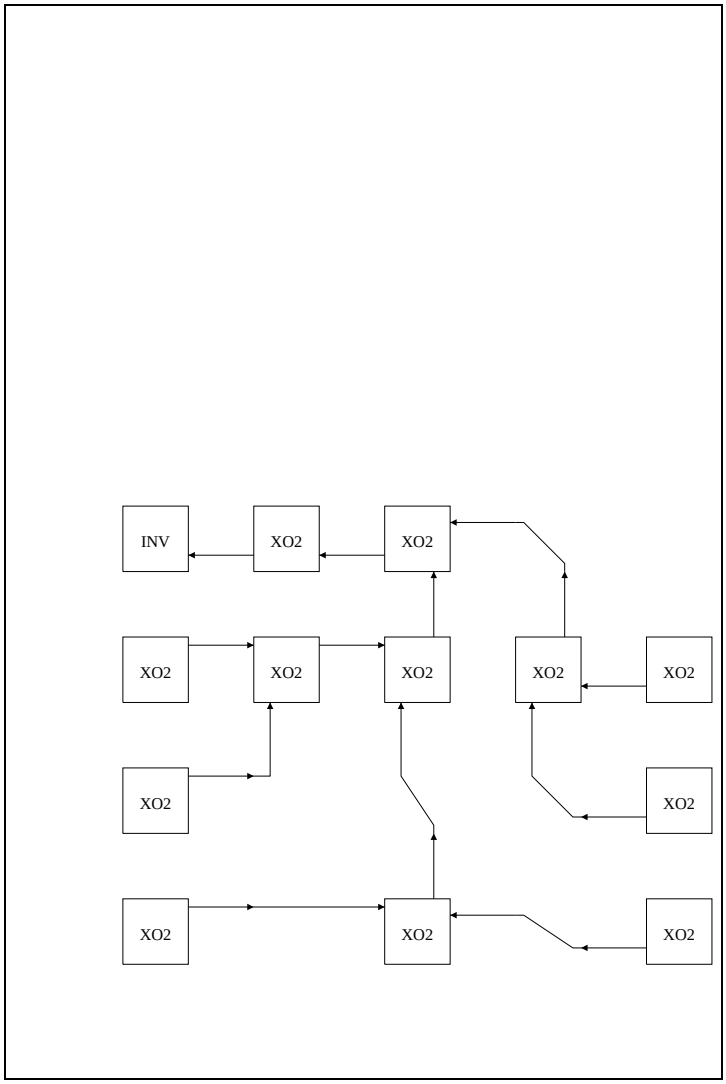
PCOE9 - 9-Bit Parity Checker Odd/Even

Layout for Shape 1



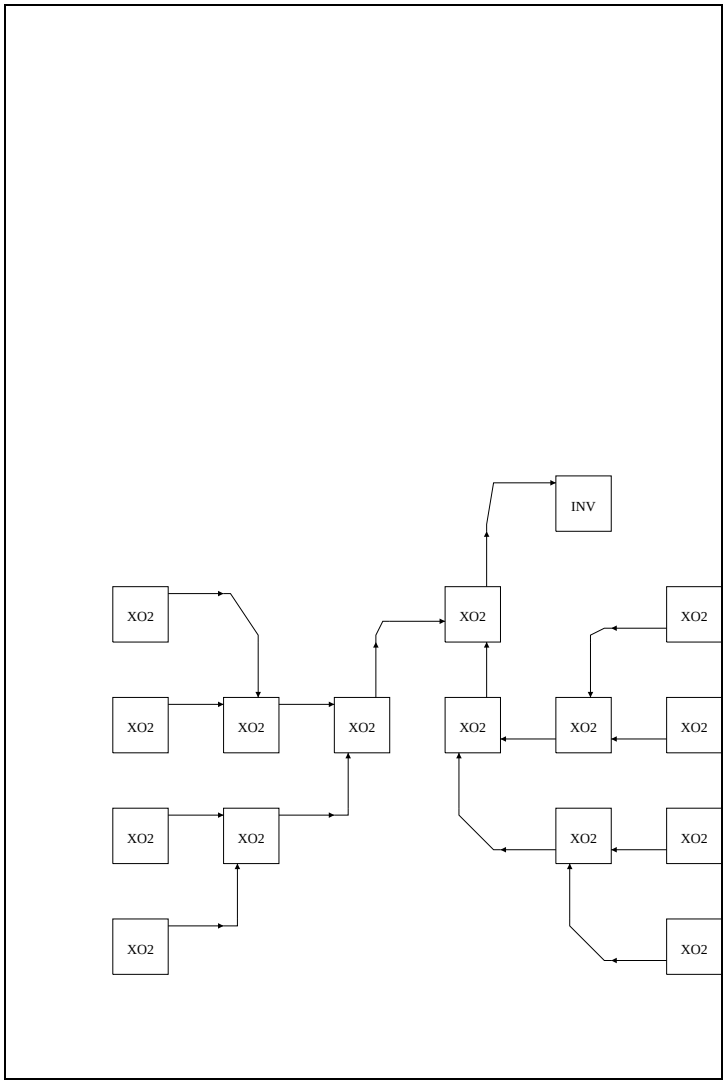
PCOE13 - 13-Bit Parity Checker Odd/Even

Layout for Shape 1



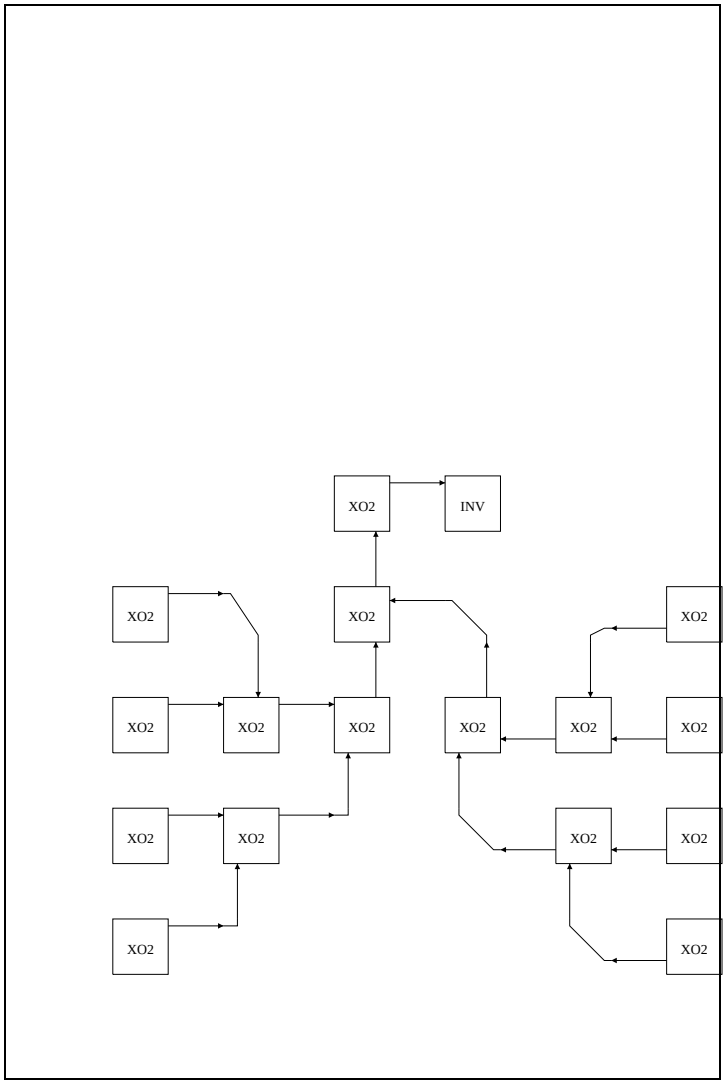
PCOE16 - 16-Bit Parity Checker Odd/Even

Layout for Shape 1



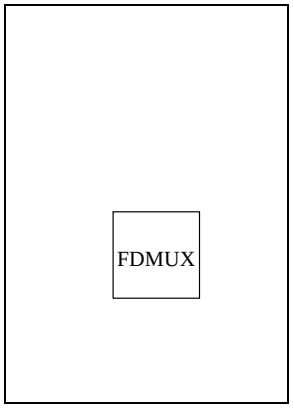
PCOE17 - 17-Bit Parity Checker Odd/Even

Layout for Shape 1



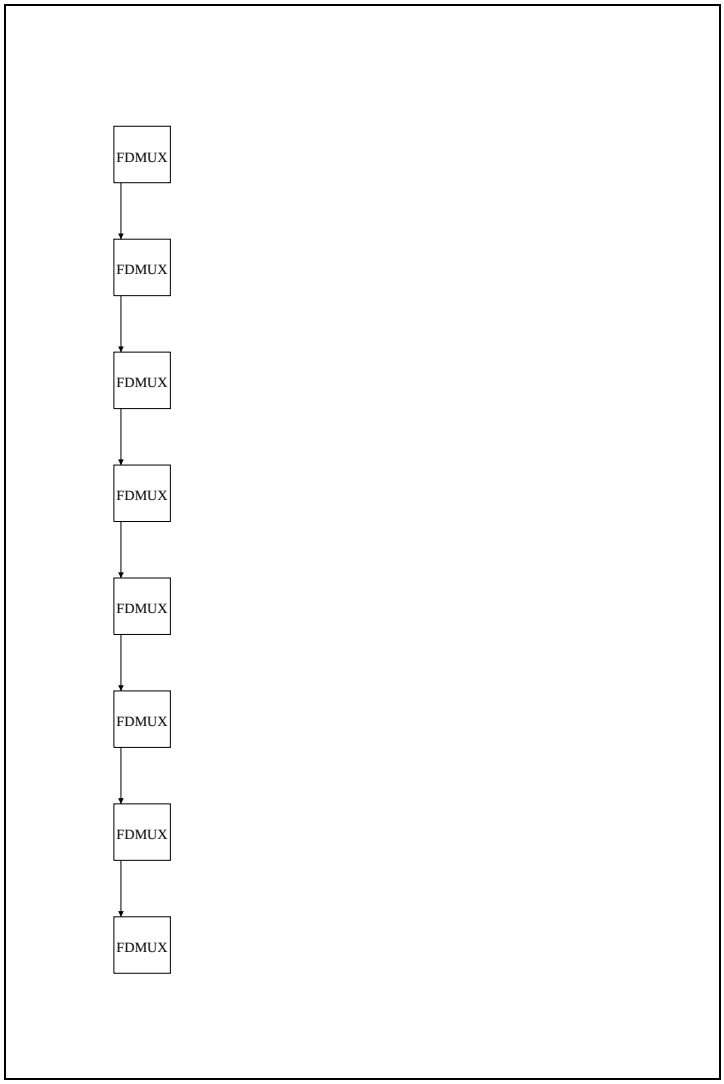
PSC1 - 1-Bit Parallel-to-Serial Converter

Layout for Shape 1



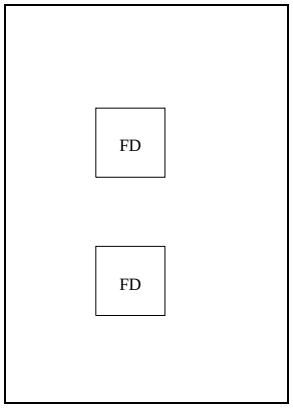
PSC8 - 8-Bit Parallel-to-Serial Converter

Layout for Shape 1



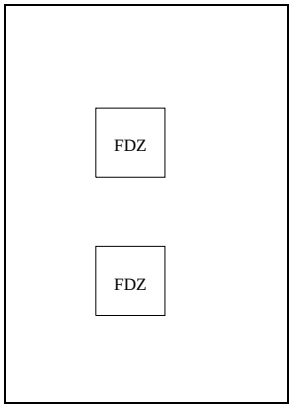
R2 - 2-Bit Register File

Layout for Shape 1



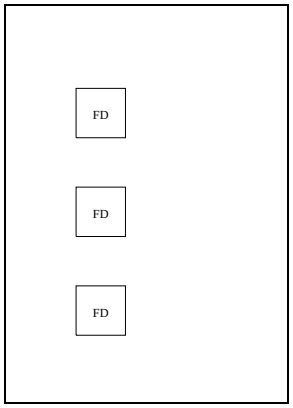
R2Z - 2-Bit Register File with Tristate Out

Layout for Shape 1



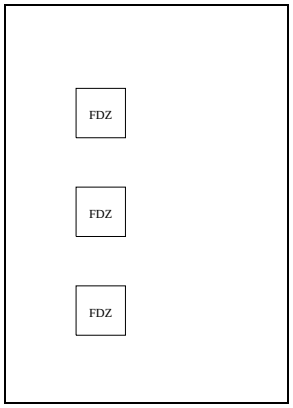
R3 - 3-Bit Register File

Layout for Shape 1



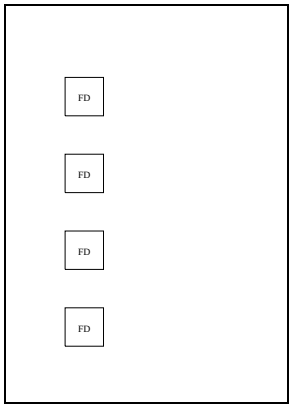
R3Z - 3-Bit Register File with Tristate Out

Layout for Shape 1



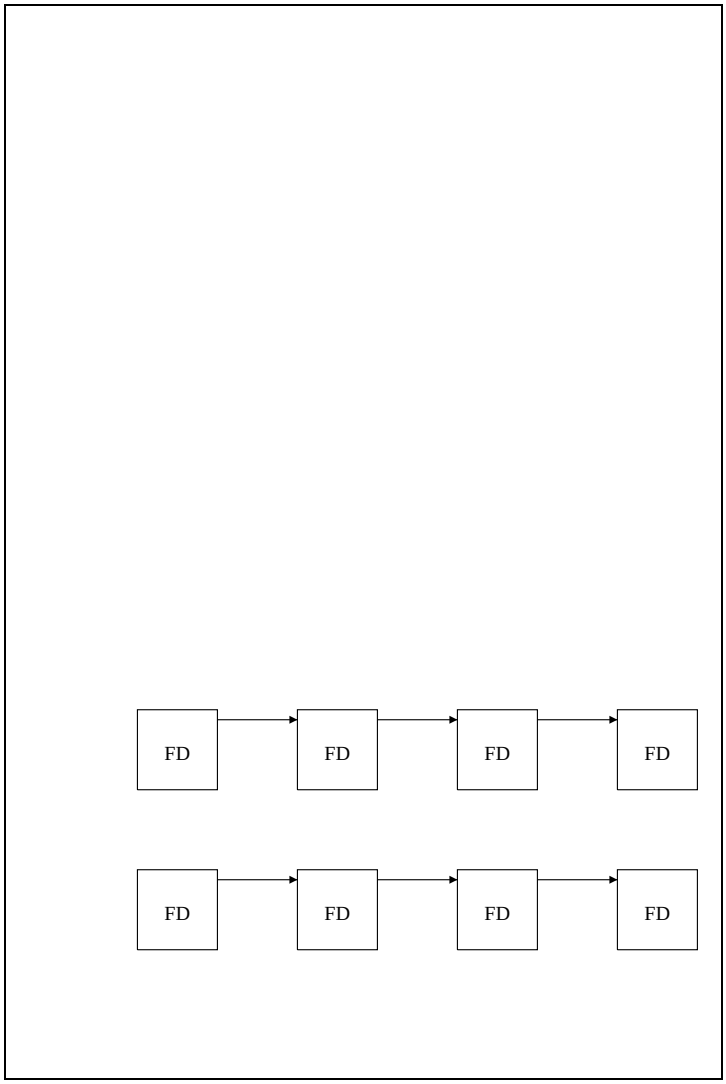
R4 - 4-Bit Register File

Layout for Shape 1



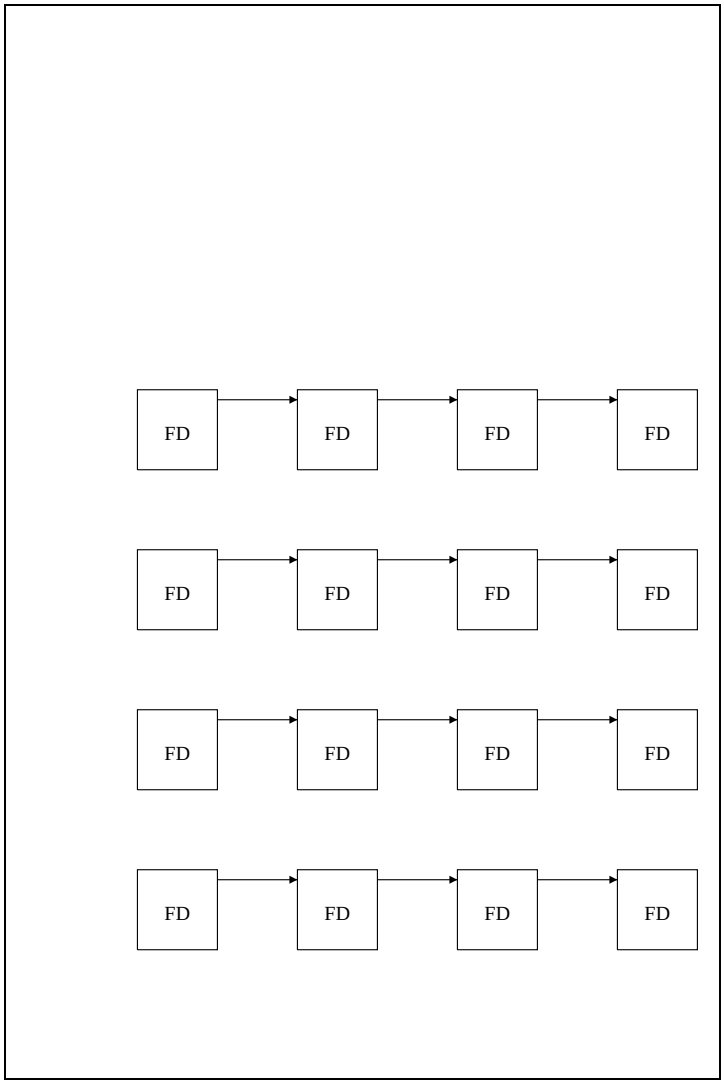
R4X2 - 4 Word x 2 Bit Register File

Layout for Shape 1



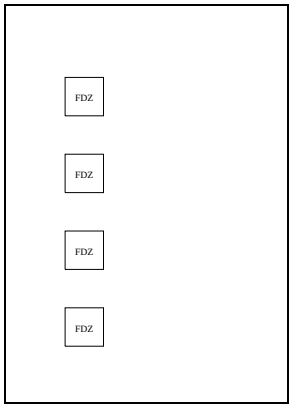
R4X4 - 4 Word x 4 Bit Register File

Layout for Shape 1



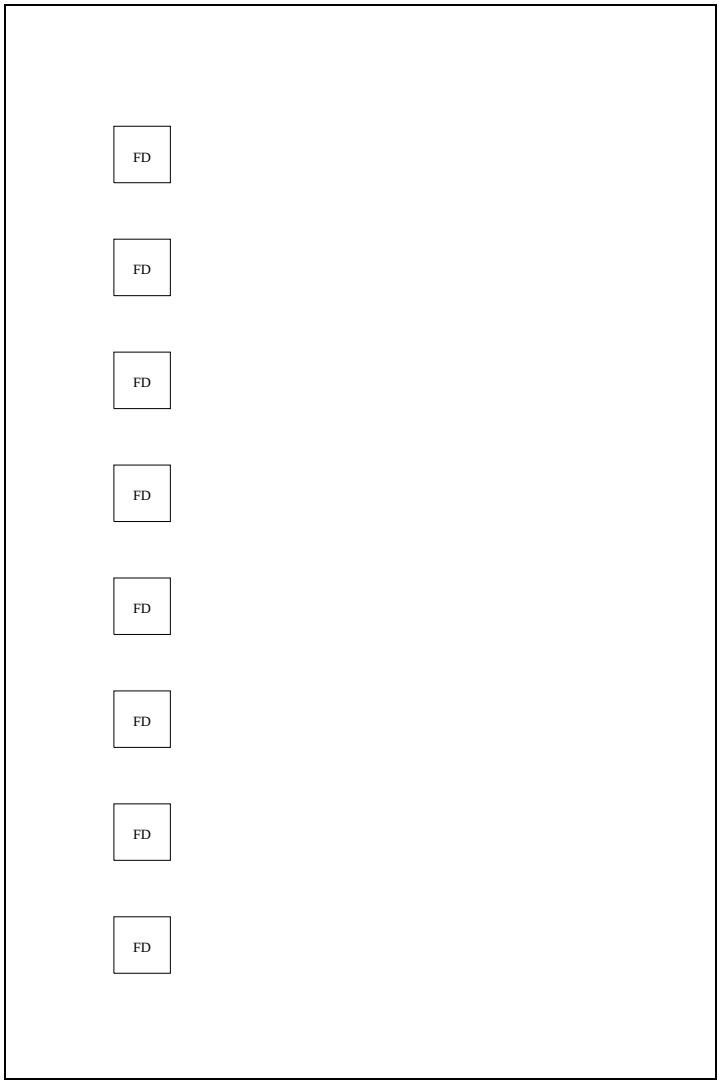
R4Z - 4-Bit Register File with Tristate Out

Layout for Shape 1



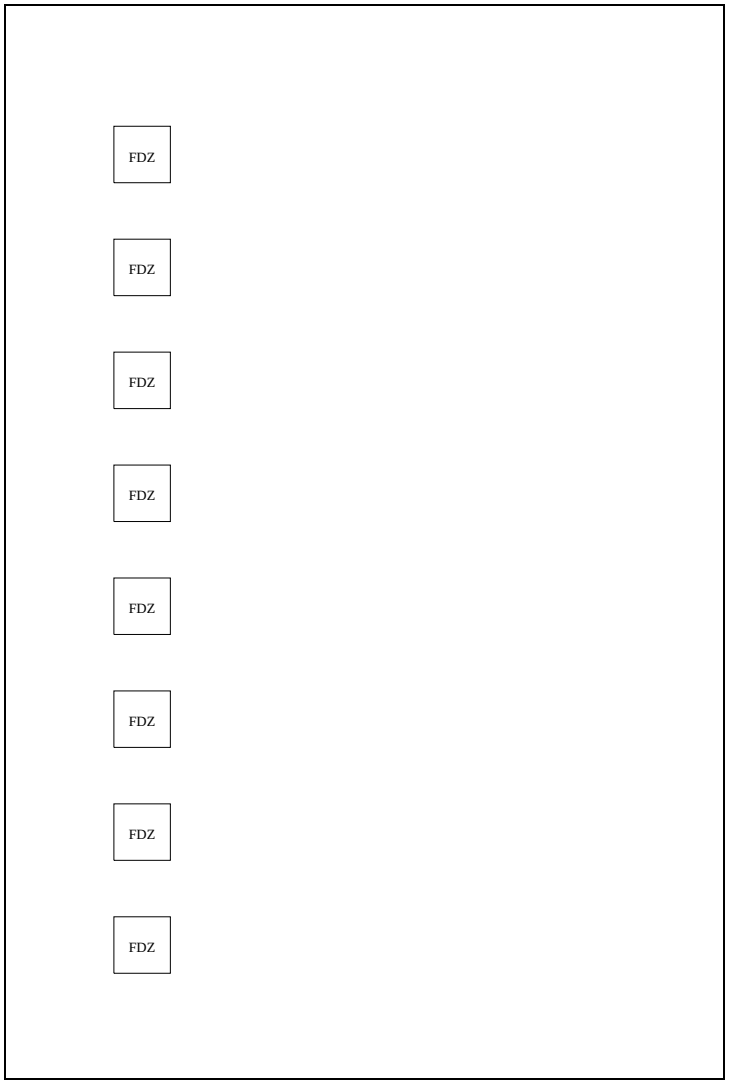
R8 - 8-Bit Register File

Layout for Shape 1



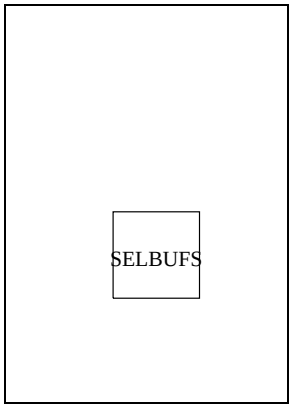
R8Z - 8-Bit Register File with Tristate Out

Layout for Shape 1



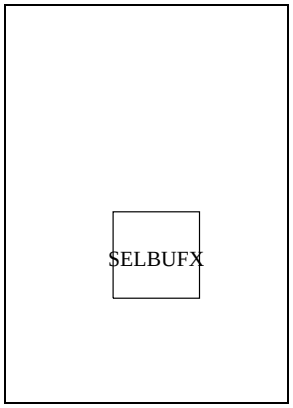
SELBUFS - Select Buffer

Layout for Shape 1



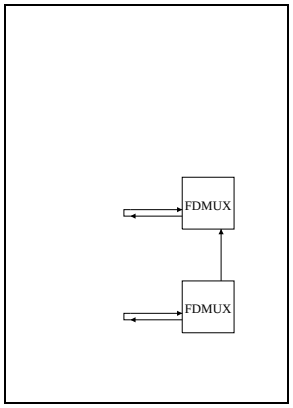
SELBUFX - Select Buffer

Layout for Shape 1



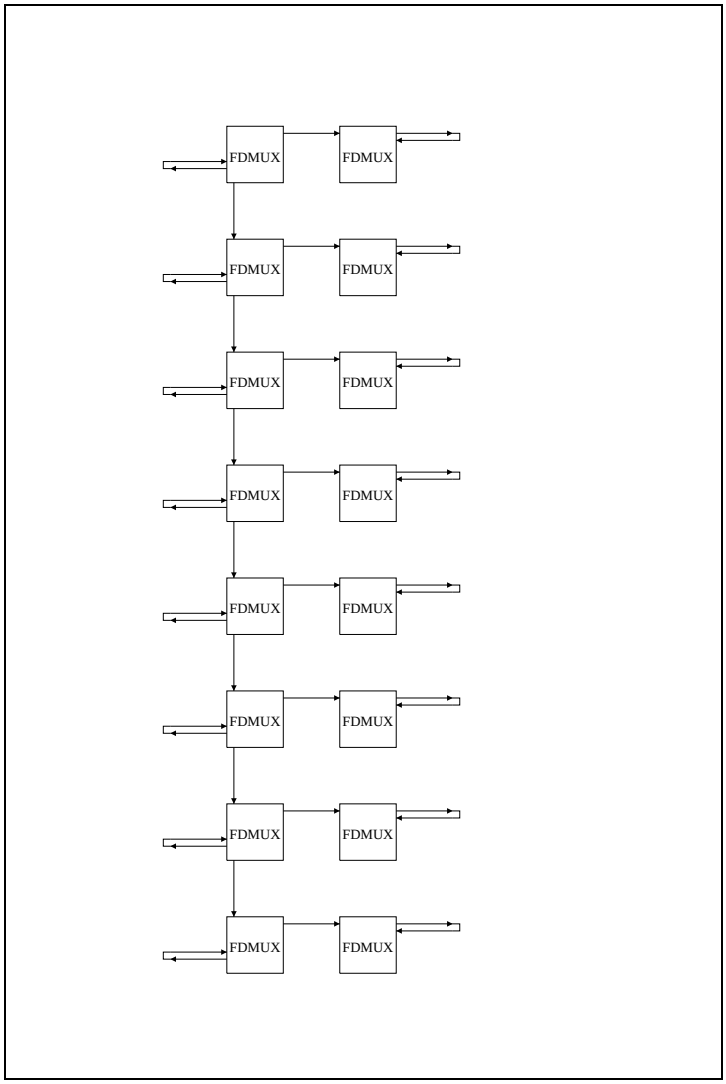
SPC1 - 1-Bit Serial-to-Parallel Converter

Layout for Shape 1



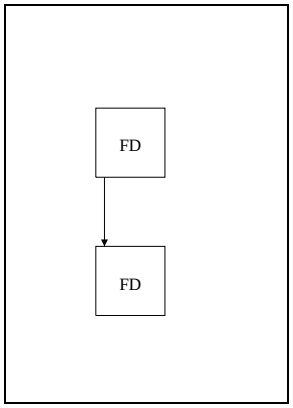
SPC8 - 8-Bit Serial-to-Parallel Converter

Layout for Shape 1



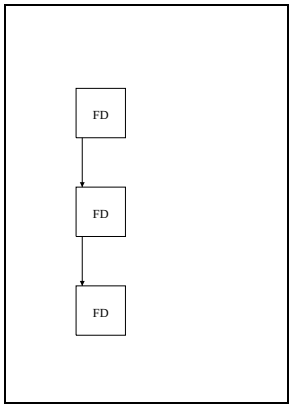
SR2 - 2-Bit Shift Register

Layout for Shape 1



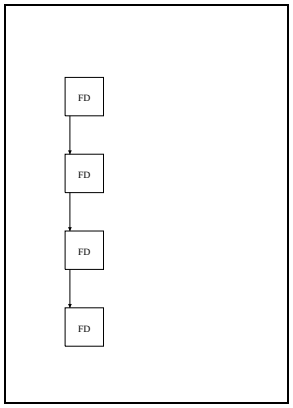
SR3 - 3-Bit Shift Register

Layout for Shape 1



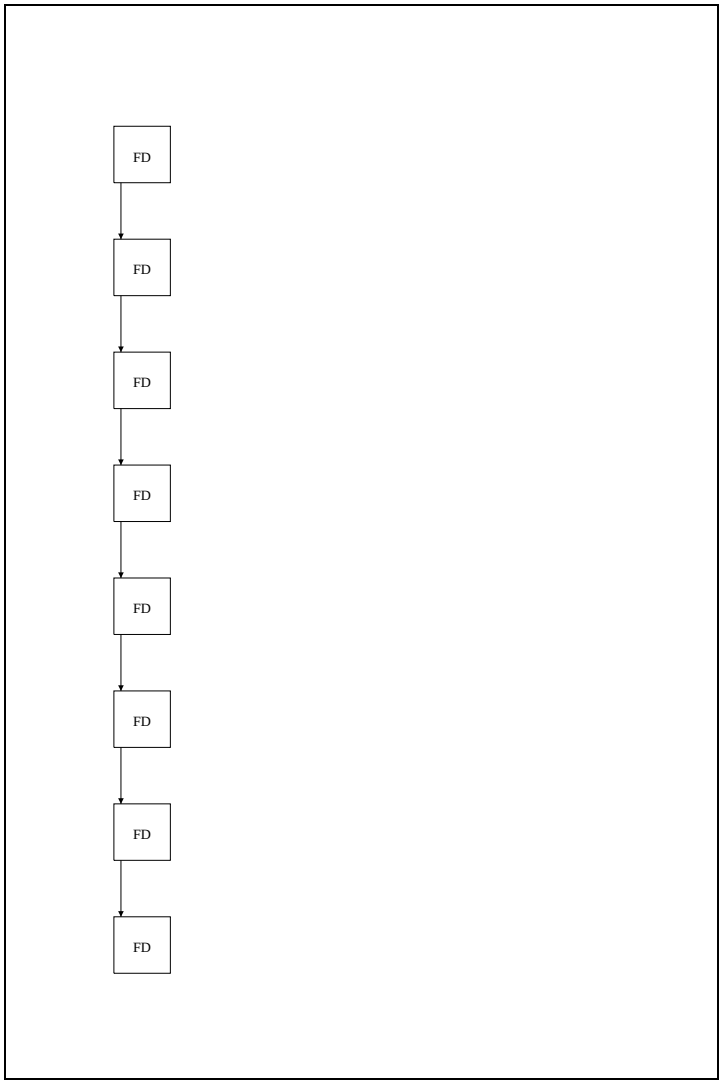
SR4 - 4-Bit Shift Register

Layout for Shape 1



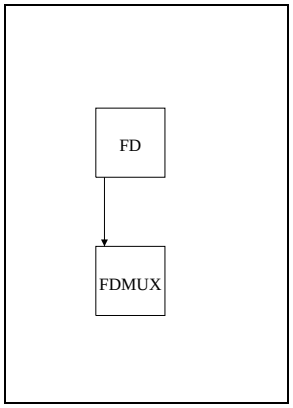
SR8 - 8-Bit Shift Register

Layout for Shape 1



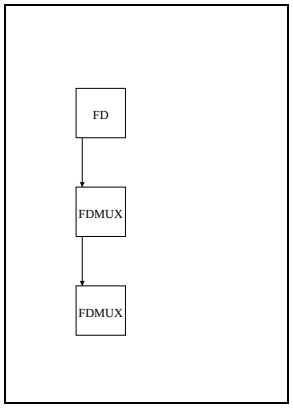
SRP2 - 2-Bit Shift Register with Parallel Load

Layout for Shape 1



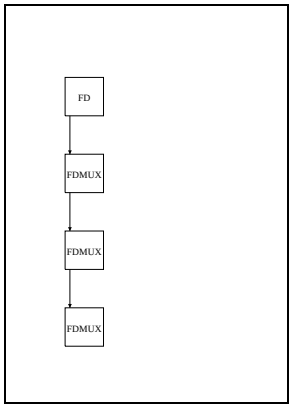
SRP3 - 3-Bit Shift Register with Parallel Load

Layout for Shape 1



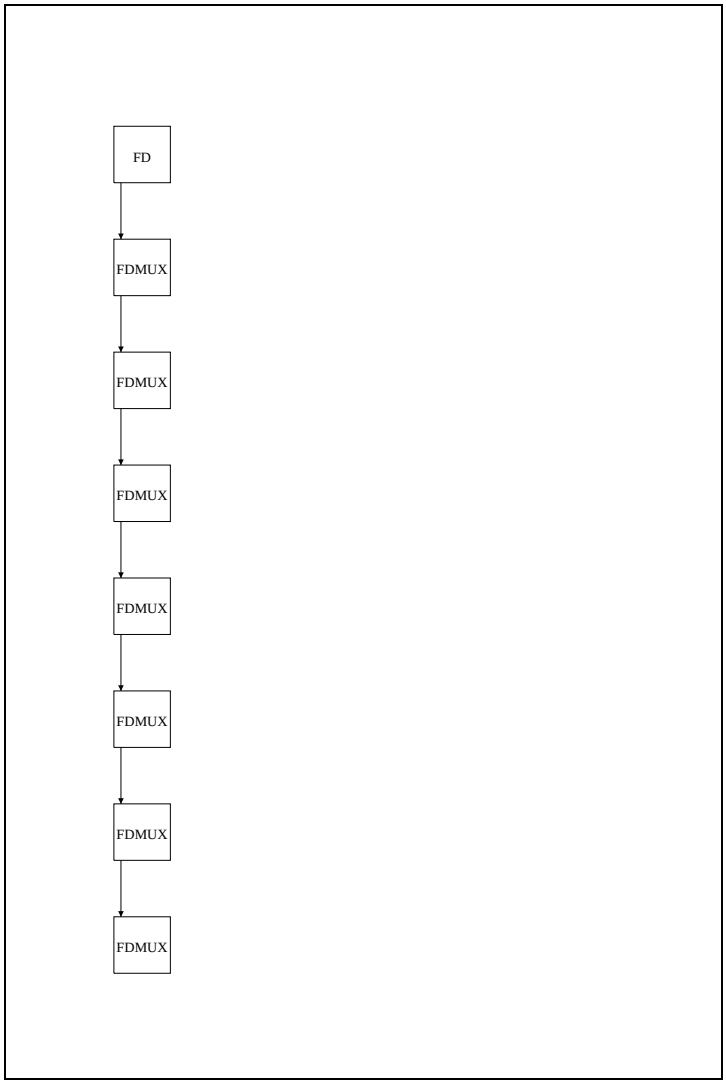
SRP4 - 4-Bit Shift Register with Parallel Load

Layout for Shape 1



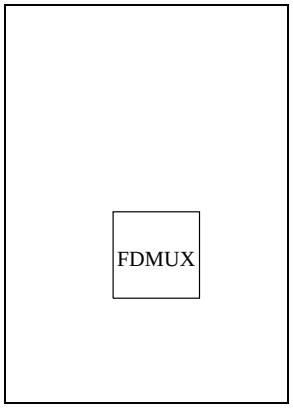
SRP8 - 8-Bit Shift Register with Parallel Load

Layout for Shape 1



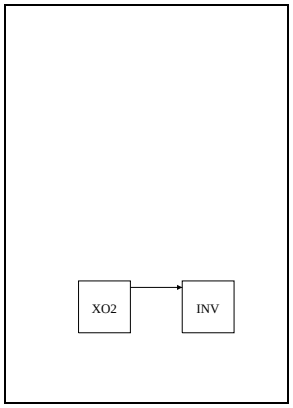
SRPST - Bit Stage Shift Register w/ Parallel Load

Layout for Shape 1



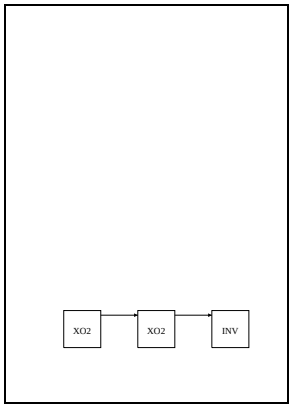
XN2 - 2-Input XNOR

Layout for Shape 1



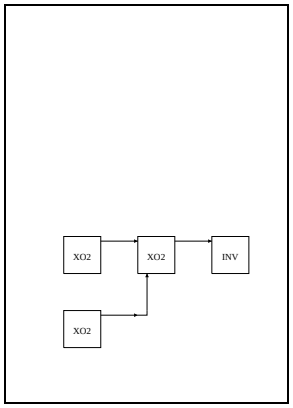
XN3 - 3-Input XNOR

Layout for Shape 1



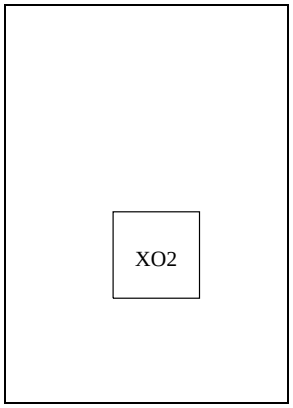
XN4 - 4-Input XNOR

Layout for Shape 1



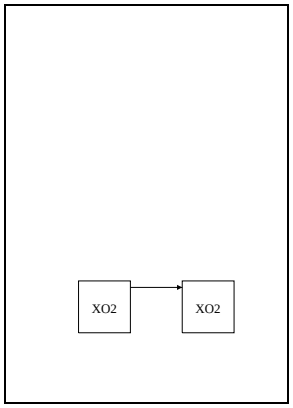
XO2 - 2-Input XOR

Layout for Shape 1



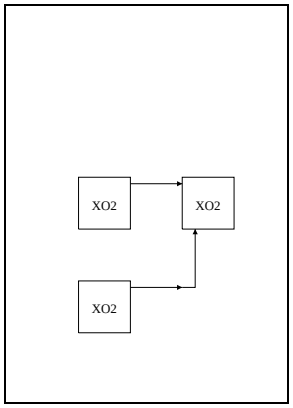
XO3 - 3-Input XOR

Layout for Shape 1



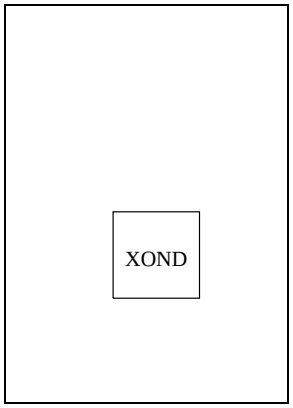
XO4 - 4-Input XOR

Layout for Shape 1



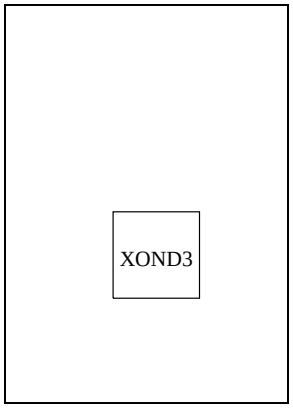
XOND - 2-Input XOR/NAND

Layout for Shape 1



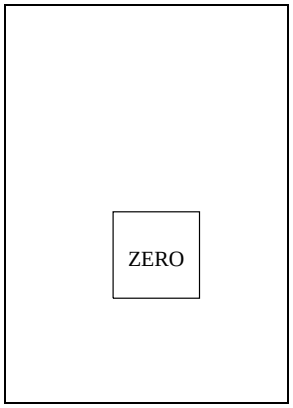
XOND3 - 2-Input XOR with 3-Input NAND

Layout for Shape 1



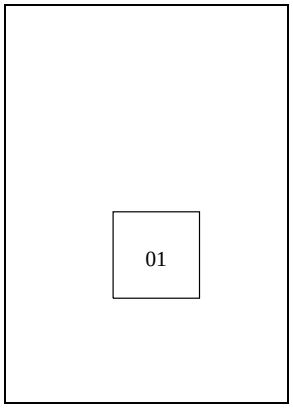
ZERO/ZEROB - Logic Zero

Layout for Shape 1



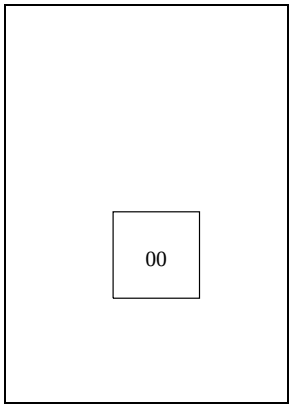
ZEROONE - Logic One and Logic Zero

Layout for Shape 1



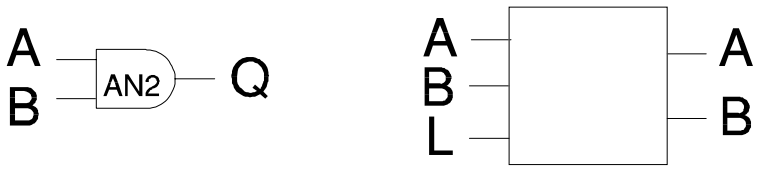
ZEROZERO - Two Logic Zeros

Layout for Shape 1



APPENDIX - Physical Layout Connections

When working with Atmel macros at the physical layout level, you should recognize that the logical connections to a macro can be realized physically in different ways. For instance, the AN2 primitive has the following logical and physical representations:



Logical **Physical**

The physical representation is identical to the one shown by the Interact layout editor. In this representation, the physical pins (A, B, L) correspond, respectively, to the red, blue, and green wires used in Interact. AN2 is described in the Appendix by the following table:

AN2, Shape 1

Logical Pins	A	B	Q
Physical Pins	A/B/L	A/B/L	A/B
	A	L	A
	A	L	B
	A	B	B
	B	L	B

The above indicates that there are four possible combinations for making physical connections to the macro. The combination, (A,L,A), indicates that if the A and L wires are used as inputs, then the A wire can be used as an output. Similarly, for the combination, (A,L,B), if the A and L wires are used as inputs, then the B wire can also be used as an output. However, if the A

and B wires are used as inputs, instead, then only the B wire can be used as output. This combination is indicated by (A,B,B).

When making macro interconnections at the layout level, you should consult this Appendix for all the possible legal combinations. Only primitives are listed in the Appendix. For a complex macro, which consists of more than one primitive, the possible interconnections can be figured out if each primitve is known. The primitives are listed in alphabetical order.

AN2, Shape 1

Logical Pins	A	B	Q
Physical Pins	A/B/L	A/B/L	A/B
	A	L	A
	A	L	B
	A	B	B
	B	L	B

AN2INV, Shape 1

Logical Pins	A	B	Q0	Q1N
Physical Pins	L	A	A	B
	L	A	A	
	L			B

AN2L, Shape 1

Logical Pins	A	BN	Q
Physical Pins	A	L	A/B
	A	L	A
	A	L	B

AN2S, Shape 1

Logical Pins	A	B	C	Q0	Q1
Physical Pins	A/L	A/L	B	A	B
	A	L		A	
		B		B	

AN2X, Shape 1

Logical Pins	A	B	C	Q0	Q1
Physical Pins	A/L	A/L	B	B	A
	A	L		B	
			B		A

AN3, Shape 1

Logical Pins	A	B	C	Q
Physical Pins	A/B/L	A/B/L	A/B/L	B
	A	B	L	B

ANXO, Shape 1

Logical Pins	A	B	C	Q
Physical Pins	A/L	B	A/L	A
	A	B	L	A
	L	B	A	A

BUFFER/BUFFERB, Shape 1

Logical Pins	A	Q
Physical Pins	A	A/B
	A	B
	A	A

BUFZ, Shape 1

Logical Pins	A	OE	Q
Physical Pins	A	B	L
	A	B	L

CLKEDGE, Shape 1

Logical Pins	Q
Physical Pins	A/L
	A
	L

CLKEDGEZ, Shape 1

Logical Pins	OE	Q
Physical Pins	B	L
	B	L

FD, Shape 1

Logical Pins	D	Q
Physical Pins	A	A/L
	A	L
	A	A

FDHA, Shape 1

Logical Pins	A	B	Q1	Q2
Physical Pins	A/B/L	A/B/L	A/L	B
	A	B	A	
	L	B	A	
	A	B	L	
	A	B		B
	L	B		B
	A	B		B

FDMUX, Shape 1

Logical Pins	D0	D1	S	Q
Physical Pins	B	A	L	A
	B	A	L	A

FDN, Shape 1

Logical Pins	DN	Q
Physical Pins	A/B/L	A/L
	A	A
	A	L
	B	A
	B	L
	L	A

FDND, Shape 1

Logical Pins	A	B	Q1N	Q0
Physical Pins	A/L	A/L	A	B
	A	L	A	
	A	L		B

FDOR, Shape 1

Logical Pins	A	B	Q
Physical Pins	L/B	L/B	A
	L	B	A

FDORL, Shape 1

Logical Pins	A	BN	Q
Physical Pins	A	L	A
	A	L	A

FDXO, Shape 1

Logical Pins	A	B	Q
Physical Pins	A/B/L	A/B/L	A/L
	A	B	A
	L	B	A
	A	B	L

FDXOAN3, Shape 1

Logical Pins	A	B	C	Q1	Q2
Physical Pins	A/L	B	A/L	A	B
	A	B	L	A	
	A	B	L		B

FDZ, Shape 1

Logical Pins	D	OE	Q
Physical Pins	A	B	A/L
	A	B	L

FDZQ, Shape 1

Logical Pins	D	OE	Q	Q0
Physical Pins	A	B	L	A
	A	B	L	
	A			A

HZ, Shape 1

Logical Pins	OE	Q
Physical Pins	B	L
	B	L

INV, Shape 1

Logical Pins	A	Q
Physical Pins	A/B/L	A/B/L
	A	A
	A	B
	A	L
	B	A
	B	B
	B	L
	L	A
	L	B

INVANZ, Shape 1

Logical Pins	A	B	Q0	Q1N
Physical Pins	A/L	L	A	B
	A	L	A	
		L		B

INVINV, Shape 1

Logical Pins	A	Q0N	Q1N
Physical Pins	A/B/L	A/B	A/B
	L	A	
	L	B	
	A	A	
	A	B	
	A	L	
	B	B	
	B	A	
	B	L	
	L		A
	L		B
	A		A
	A		B
	A		L
	B		B
	B		A
	B		L

LZ, Shape 1

Logical Pins	OE	QN
Physical Pins	B	L
	B	L

MUX, Shape 1

Logical Pins	D0	D1	S	Q
Physical Pins	B	A	L	A
	B	A	L	A

ND2, Shape 1

Logical Pins	A	B	QN
Physical Pins	A/B/L	A/B/L	A/B
	B	L	B
	A	L	A
	A	L	B
	A	B	B

ND3, Shape 1

Logical Pins	A	B	C	Q
Physical Pins	A/B/L	A/B/L	A/B/L	B
	A	B	L	B

NDND, Shape 1

Logical Pins	A	B	Q0N	Q1N
Physical Pins	A/L	A/L	A/B	A/B
	A	L	A	
	A	L	B	
	A	L		A
	A	L		B

ONE/ONEB, Shape 1

Logical Pins	Q
Physical Pins	A/B/L

ONEONE, Shape 1

Logical Pins	OUT0	OUT1
Physical Pins	A/L	B
	A	
	L	
		B

ORL, Shape 1

Logical Pins	A	BN	Q
Physical Pins	A	L	A
	A	L	A

ORT, Shape 1

Logical Pins	A	B	Q
Physical Pins	B/L	B/L	A
	B	L	A

SELBUFS, Shape 1

Logical Pins	A	B	C	Q1	Q2
Physical Pins	A	B	L	A	B
	A		L	A	
		B	L		B

SELBUFX, Shape 1

Logical Pins	A	B	C	Q1	Q2
Physical Pins	A	B	L	B	A
	A		L	B	
		B	L		A

XOND, Shape 1

Logical Pins	A	B	Q0	Q0N
Physical Pins	A/B/L	A/B/L	A/L	B
	A	B	L	
	A	B	A	
	L	B	A	
	A	B		B
	A	B		B
	L	B		B

XOND3, Shape 1

Logical Pins	A	B	C	Q1	Q2N
Physical Pins	A/L	B	A/L	A	B
	A	B	L	A	
	A	B	L		B

XOR2, Shape 1

Logical Pins	A	B	Q
Physical Pins	A/B/L	A/B/L	A/B/L
	A	B	L
	A	B	A
	L	B	A

ZERO/ZEROB, Shape 1

Logical Pins	QN
Physical Pins	A/B/L

ZEROONE, Shape 1

Logical Pins	HI	LO
Physical Pins	A/B/L	A/B/L
	A	
	B	
	L	
		A
		B
		L

ZEROZERO, Shape 1

Logical Pins	OUT0	OUT1
Physical Pins	A/L	B
	A	
	L	
		B