AT40K Macro Library

June 2002

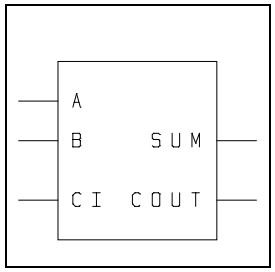
Macro Library

Introduction

This book explains the macro library for the AT40K family of FPGAs. The AT40K library of components can be divided into 2 types of macros: functional and dynamic. Functional macros are components with fixed functionality, such as the 2 input AND gate. Dynamic macros are designed to allow user specification of any desired functionality attached as an attribute, via an equation string, on the symbol. This should be used only when a specific function for an AT40K core cell is required. Designs targeted to AT40K can use a mix of dynamic and functional macros.

FA

Full adder



Truth Table

Input			Output	
A	B	CI	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
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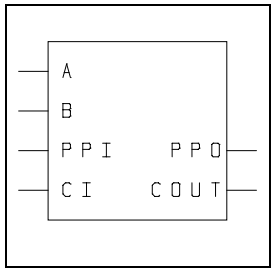
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

MULT

Multiplier



Truth Table

Input				Output	
A	B	PPI	CI	PPO	COUT
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0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
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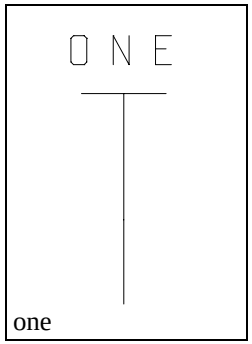
1	1	1	0	0	1
1	1	1	1	1	1

ONE

Constant One



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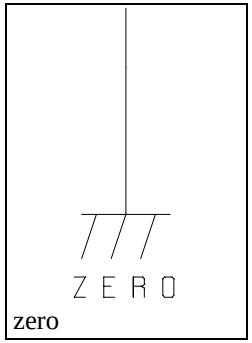

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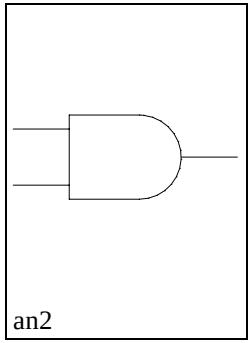
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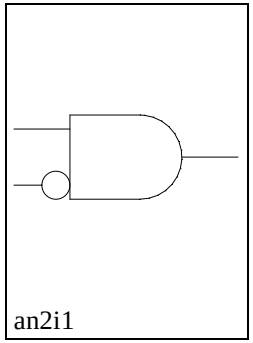
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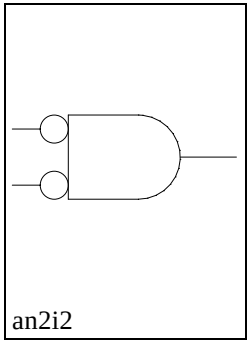
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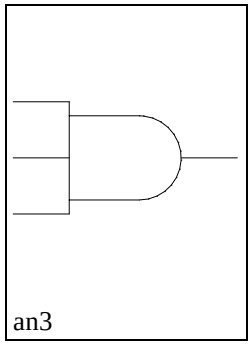
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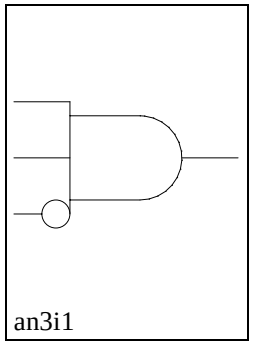
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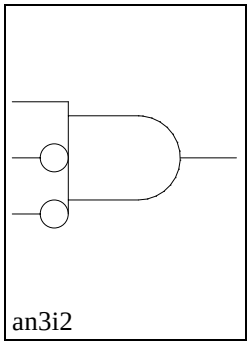
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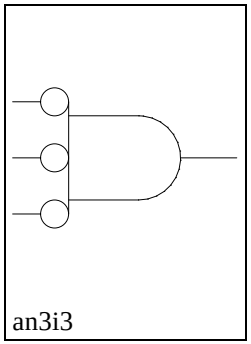
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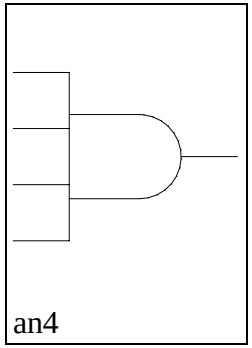
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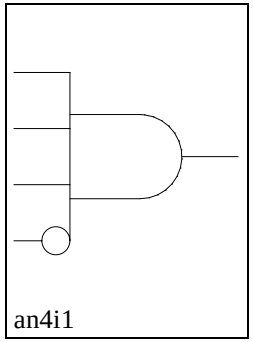
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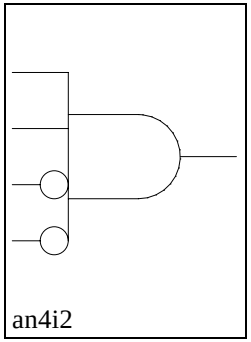
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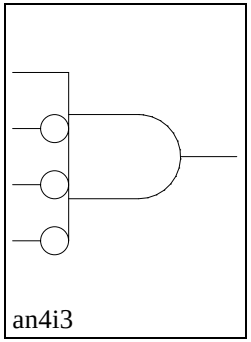
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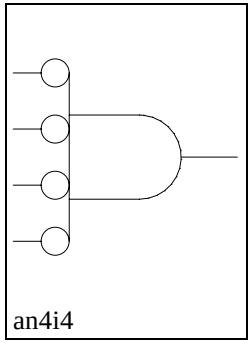
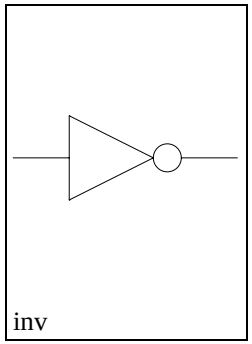


Inverter



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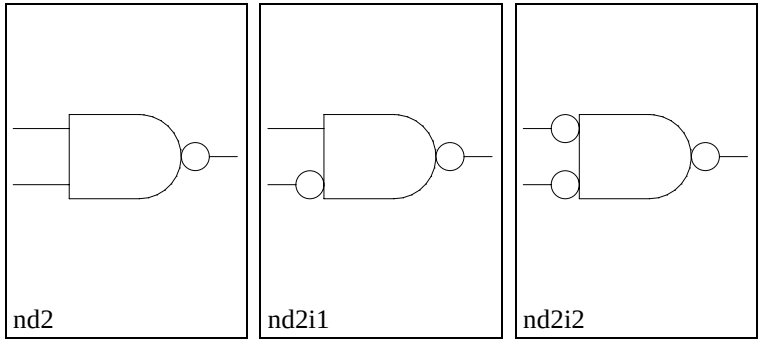

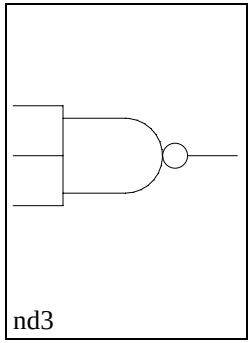
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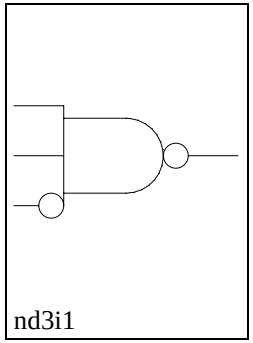
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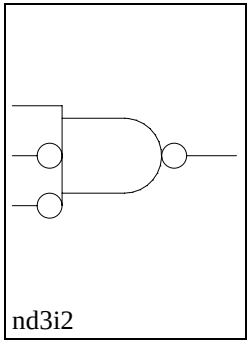
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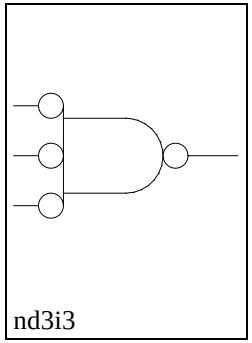
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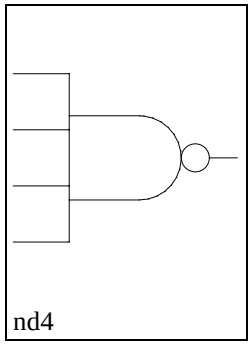
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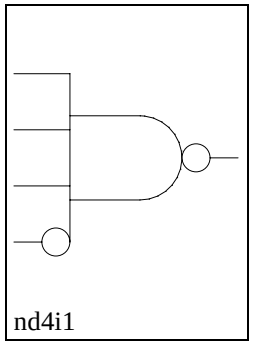
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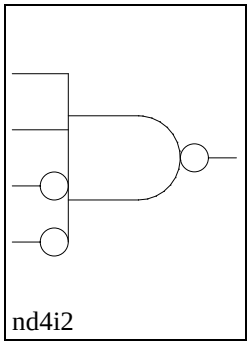
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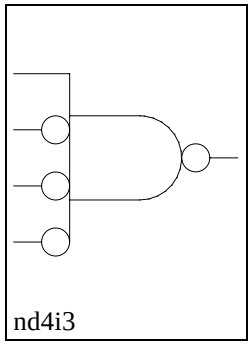
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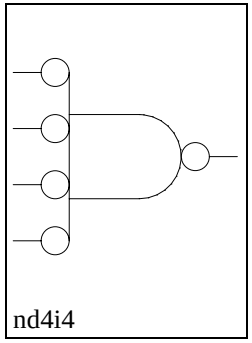
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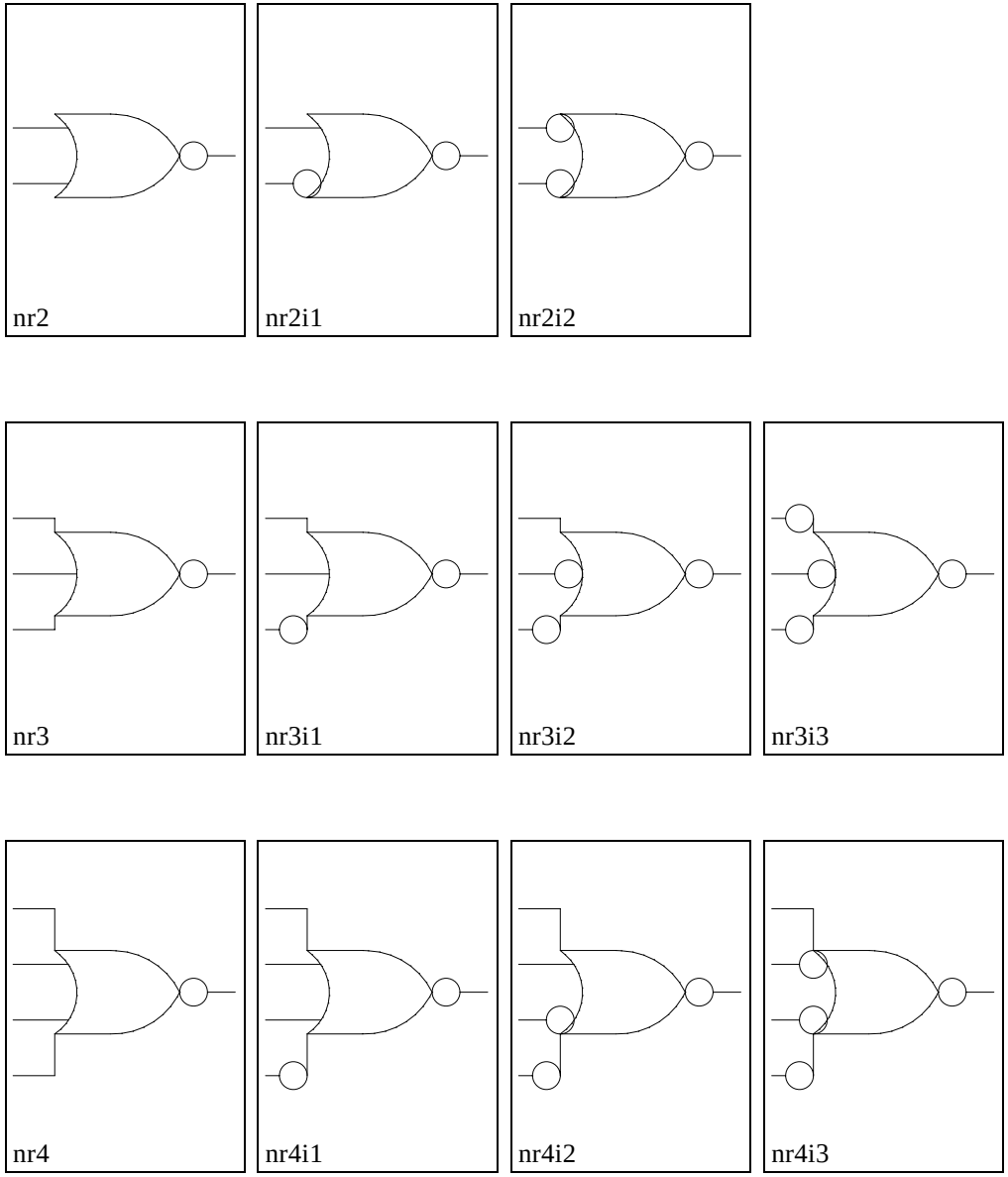

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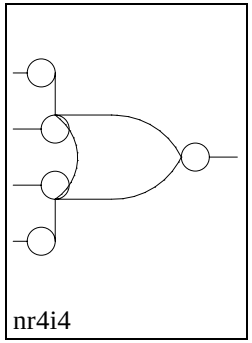
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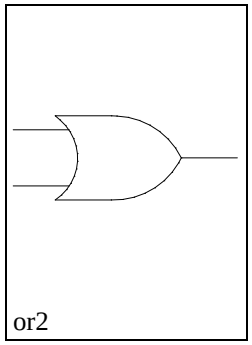
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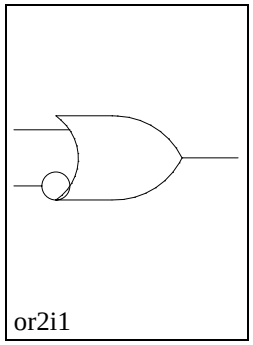
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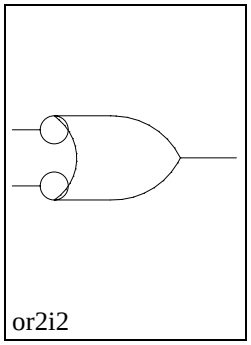
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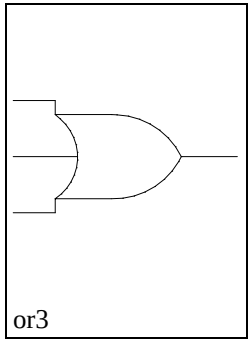
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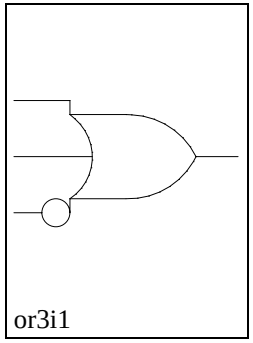
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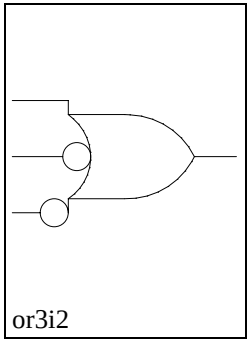
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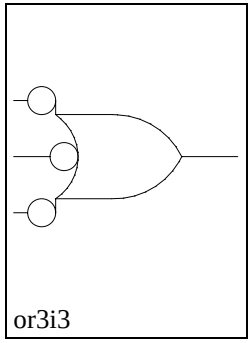
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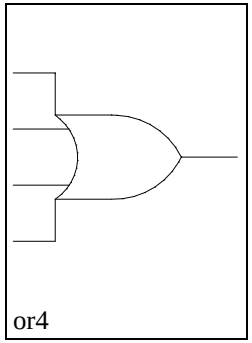
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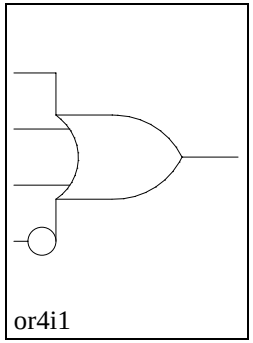
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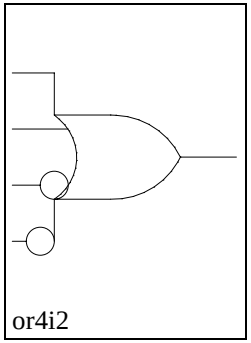
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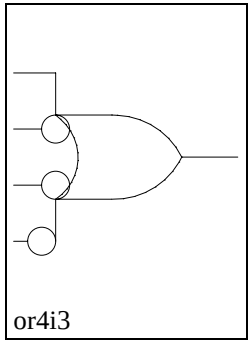
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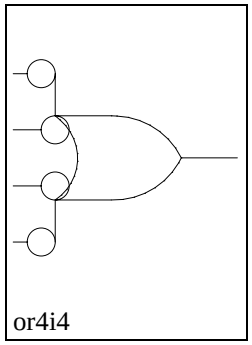
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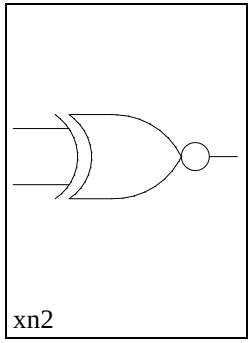
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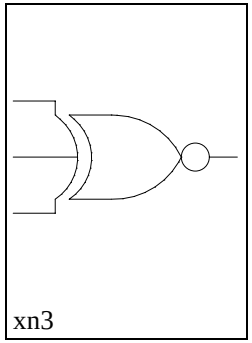
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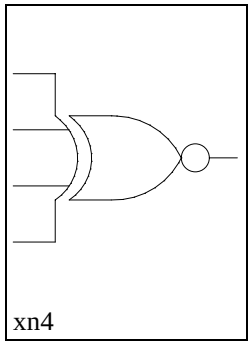
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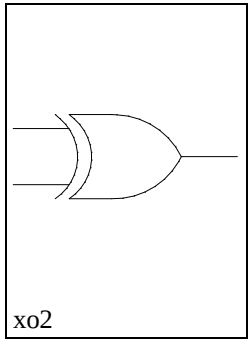
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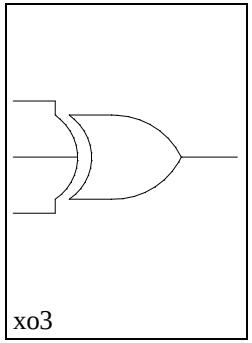
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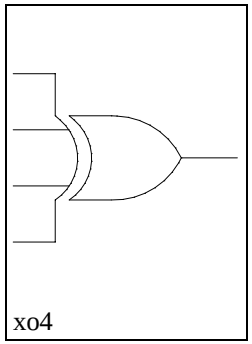

xo4

I/O Attributes

This section covers the I/O macros available for the AT40K. In order to specify additional functionality on the I/O, various properties or attributes are used. Different pre-defined attributes can be set on the I/O pads in the AT40K library. Attributes are used on the I/O macros to select the threshold levels, different slew rates etc. The pre-defined attributes that can be specified on the I/O macros are listed below:

THRESHOLD
SCHMITT
SLEWRATE
EXTRADELAY

THRESHOLD

Description

Specifies the threshold level on the input buffers.

Value	Explanation
CMOS	CMOS on input
TTL	TTL on input

SCHMITT

Description

Specifies whether a Schmitt trigger circuit on the input pads should be enabled or disabled. The Schmitt trigger is a regenerative comparator circuit to improve the rise and fall times (leading and trailing edges) of the incoming signal.

Value	Explanation
ENABLE	Enable the Schmitt trigger circuit
DISABLE	Disable the Schmitt trigger circuit

SLEWRATE

Description

Specifies the output drive.

Value	Explanation
FAST	Full drive (20 mA buffer)
MEDIUM	Medium drive (14 mA buffer)
SLOW	Standard drive (6 mA buffer)

EXTRADELAY

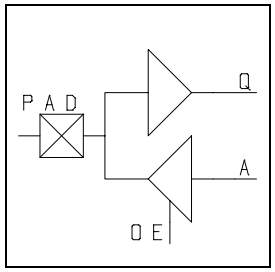
Description

The input buffers in the AT40K library can have four different intrinsic delays. This attribute lets the user specify an extra delay on the input signal to meet any data hold requirements. A value of ‘0’ provides no extra delay above the intrinsic delay of the input buffer and a value of ‘1’ allows an extra delay of approximately 1ns above the intrinsic delay.

Value	Explanation
0	No extra intrinsic delay
1	Extra intrinsic delay of approx. 1ns
3	Extra intrinsic delay of approx. 3ns
5	Extra intrinsic delay of approx. 5 ns

BIBUF

Bidirectional buffer



Truth Table

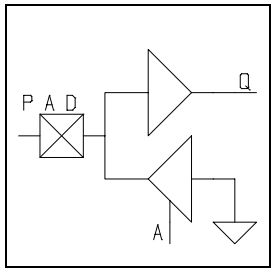
Input		Output	
A	**OE**	**PAD**	**Q**
a	1	a	a
-	0	z	pad

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the input
SLEWRATE	Yes	FAST	Output drive

BIBUFOD

Bidirectional buffer open drain



Truth Table

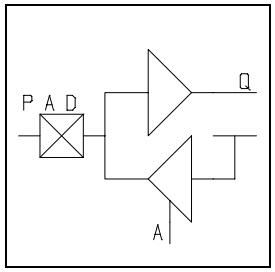
Input A	Output PAD	Q
1	0	0
0	z	pad

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the input
SLEWRATE	Yes	FAST	Output drive

BIBUFOS

Bidirectional buffer open source



Truth Table

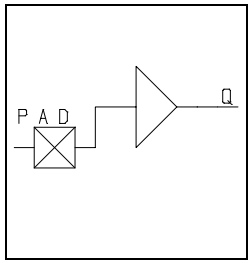
Input A	Output PAD	Q
1	1	1
0	z	pad

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the input
SLEWRATE	Yes	FAST	Output drive

IBUF

Input buffer



Truth Table

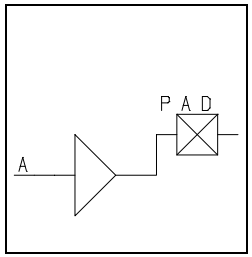
Input PAD	Output Q
0	0
1	1

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra intrinsic delay

OBUF

Output buffer



Truth Table

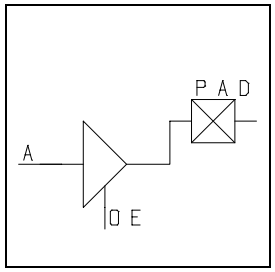
Input A	Output PAD
0	0
1	1

Attributes

Attribute	Required	Default Value	Description
SLEWRATE	Yes	FAST	Output drive

OBUFE

Output buffer with enable



Truth Table

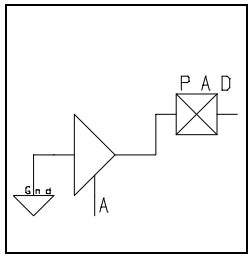
Input A	OE	Output PAD
a	1	a
-	0	z

Attributes

Attribute	Required	Default Value	Description
SLEWRATE	Yes	FAST	Output drive

OBUFOD

Output buffer open drain



Truth Table

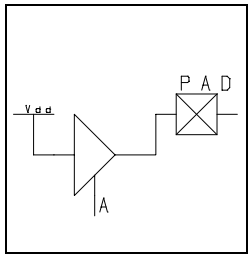
Input A	Output PAD
0	z
1	0

Attributes

Attribute	Required	Default Value	Description
SLEWRATE	Yes	FAST	Output drive

OBUFOS

Output buffer open source



Truth Table

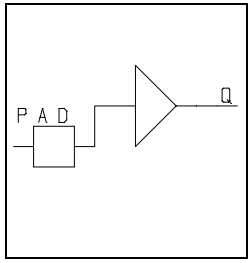
Input A	Output PAD
0	z
1	1

Attributes

Attribute	Required	Default Value	Description
SLEWRATE	Yes	FAST	Output drive

FCLKBUF

Fast clock buffer. This buffer should be specified when any of the available fast clock pads on the FPGA are used by a clock signal. Any clock signal connected to this pad will be routed to either the first or last column of the chip. A maximum of 2 fast clock buffers can be used on a single chip.



Truth Table

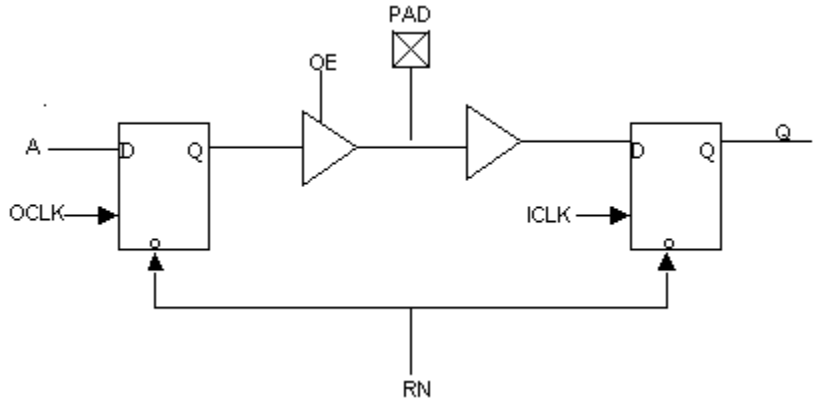
Input PAD	Output Q
0	0
1	1

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra intrinsic delay

BIBUFRR

Input : ICLK,OCLK,OE,RN,A
Output: Q
Bi-directional: PAD



Reading the input data into the device

Input			***Output***
PAD	**ICLK**	**RN**	**Q**
DATA_IN	Rising edge	0	0
DATA_IN	Rising edge	1	DATA_IN registered

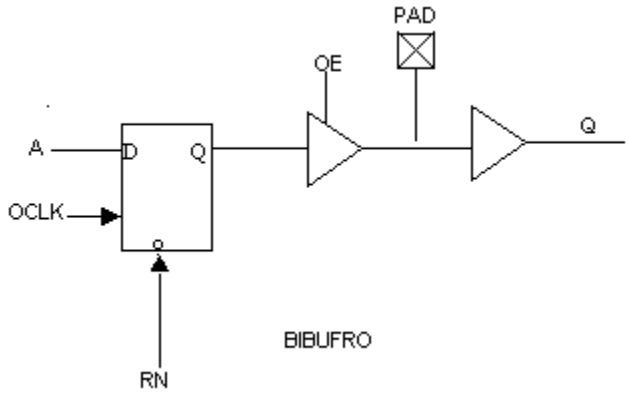
Reading the output data from the device

Input				***Output***
A	**OCLK**	**R**	**OE**	**PAD**
-	-	-	0	"Z"
DATA_OUT	Rising edge	0	1	0
DATA_OUT	Rising Edge	1	1	DATA_OUT registered

Attributes:

Attribute	**Required**	**Default Value**	**Description**
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	Enable	Enable the Schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the Input
SLEWRATE	Yes	Fast	Output drive

BIBUFRO
Input : OCLK,OE,RN,A
Output: Q
Bi-directional: PAD



Reading the input data into the device

Input	***Output***
PAD	**Q**
DATA_IN	DATA_IN

Reading the output data from the device

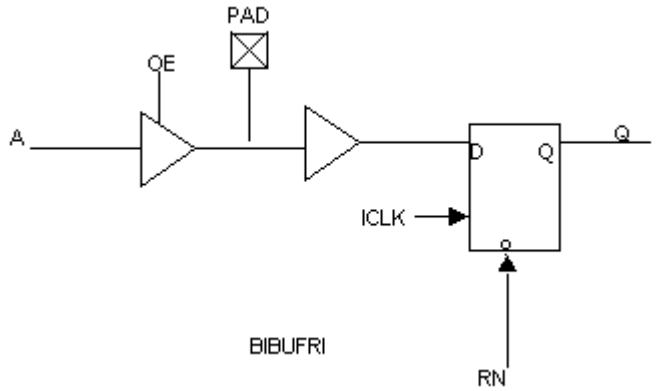
Input				***Output***
A	**OCLK**	**RN**	**OE**	**PAD**
-	-	-	0	"Z"
DATA_OUT	Rising edge	0	1	0
DATA_OUT	Rising Edge	1	1	DATA_OUT registered

Attributes:

Attribute	**Required**	**Default Value**	**Description**
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	Enable	Enable the Schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the Input
SLEWRATE	Yes	Fast	Output drive

BIBUFRI

Input : ICLK,OE,RN,A
Output: Q
Bi-directional: PAD



Reading the input data into the device

Input			***Output***
PAD	**ICLK**	**RN**	**Q**
DATA_IN	Rising edge	0	0
DATA_IN	Rising edge	1	DATA_IN registered

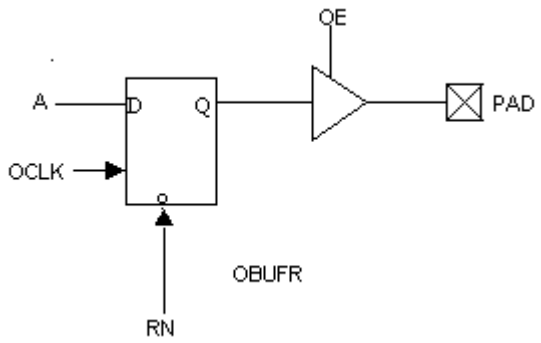
Reading the output data from the device

Input		***Output***
A	**OE**	**PAD**
DATA_OUT	0	"Z"
DATA_OUT	1	DATA_OUT

Attributes:

Attribute	**Required**	**Default Value**	**Description**
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	Enable	Enable the Schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the Input
SLEWRATE	Yes	Fast	Output drive

OBUFR
Input : OCLK,OE,RN,A
Output: PAD



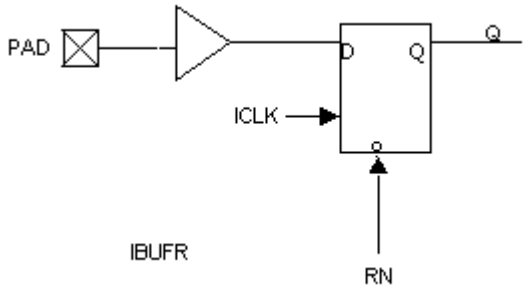
Reading the output data from the device

Input				***Output***
A	**OCLK**	**RN**	**OE**	**PAD**
-	-	-	0	"Z"
DATA_OUT	Rising edge	0	1	0
DATA_OUT	Rising Edge	1	1	DATA_OUT registered

Attributes:

Attribute	**Required**	**Default Value**	**Description**
SLEWRATE	Yes	Fast	Output drive

IBUFR
Input : ICLK,,RN,PAD
Output: Q



Reading the input data into the device

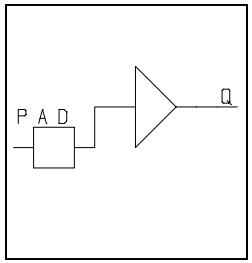
Input			***Output***
PAD	**ICLK**	**RN**	**Q**
DATA_IN	Rising edge	0	0
DATA_IN	Rising edge	1	DATA_IN registered

Attributes:

Attribute	**Required**	**Default Value**	**Description**
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	Enable	Enable the Schmitt trigger
EXTRADELAY	Yes	0	Extra delay on the Input

GCLKBUF

Global clock buffer. This buffer should be used to bring any clock signal to the global clock routing resources of the chip. A maximum of 8 global clocks are available for the FPGA.



Truth Table

Input PAD	Output Q
0	0
1	1

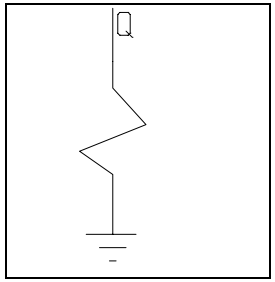
Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra intrinsic delay

IOPULLDN

This component is a resistor which provides a weak 0 at its output. It can be connected to input pads, open drain and tri-state output pads to ensure a logic low level when all the drivers are off.

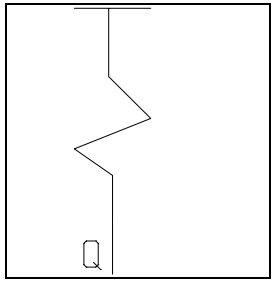
Note: IOPULLDN components cannot be connected to any internal nodes of the design.



IOPULLUP

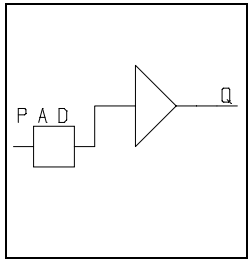
This component is a resistor which provides a weak 1 at its output. It can be connected to input pads, open drain and tri-state output pads to ensure a logic high level when all the drivers are off.

Note: IOPULLUP components cannot be connected to any internal nodes of the design.



RSBUF

Global set/reset buffer. This buffer should be used to bring the set/reset signal to the global set/reset routing resource of the chip. Only 1 such buffer is allowed in a design



Truth Table

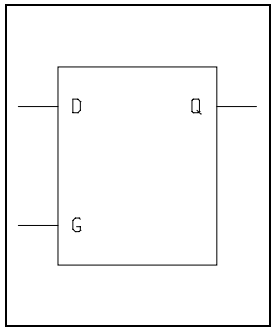
Input PAD	Output Q
0	0
1	1

Attributes

Attribute	Required	Default Value	Description
THRESHOLD	Yes	CMOS	CMOS on Input
SCHMITT	Yes	ENABLE	Enable the schmitt trigger
EXTRADELAY	Yes	0	Extra intrinsic delay

LD

Latch

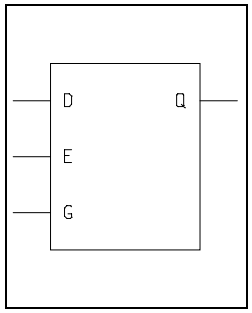


Truth Table

Input		Output
D	G	Q
x	0	q
d	1	d

LDE

Latch with enable

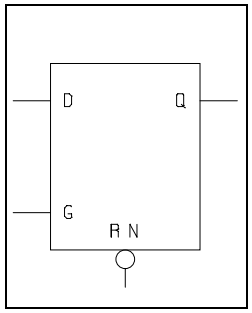


Truth Table

Input D	E	G	Output Q
x	x	0	q
x	0	1	q
d	1	1	d

LDRA

Latch with reset

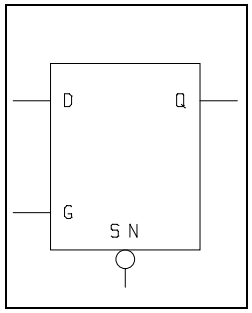


Truth Table

Input D	G	RN	Output Q
x	x	0	0
x	0	1	q
d	1	1	d

LDSA

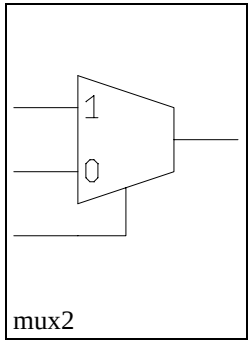
Latch with set



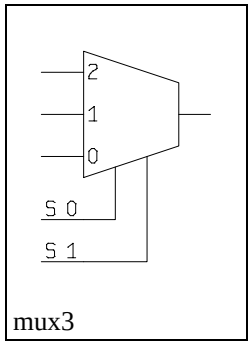
Truth Table

Input			Output
D	G	SN	Q
x	x	0	1
x	0	1	q
d	1	1	d

Multiplexor



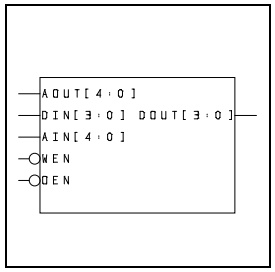
mux2



mux3

RAMD

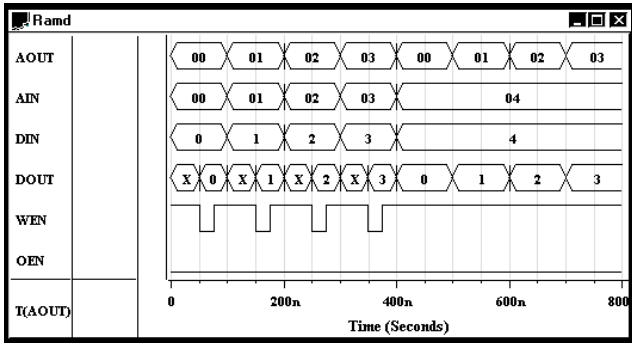
32 X 4 asynchronous dual port RAM



Pins

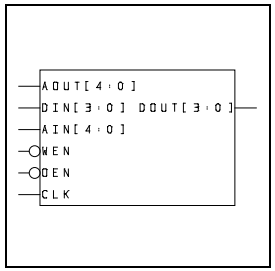
Pin	Description
AOUT[4:0]	Read address bus
AIN[4:0]	Write address bus
DOUT[3:0]	Data output bus
DIN[3:0]	Data Input bus
WEN	Active low write enable
OEN	Active low output enable

Timing Diagram



RAMDSYNC

32 X 4 synchronous dual port RAM



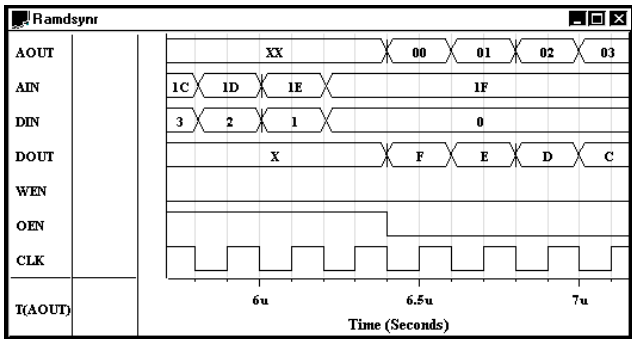
Pins

Pin	Description
AOUT[4:0]	Read address bus
AIN[4:0]	Write address bus
DOUT[3:0]	Data output bus
DIN[3:0]	Data Input bus
CLK	Clock
WEN	Active low write enable
OEN	Active low output enable

Attributes

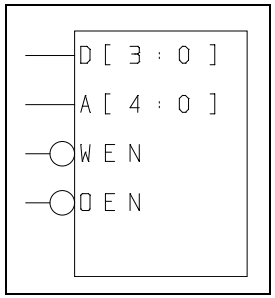
Attribute	Required	Default Value	Description
CLOCKEDGE	Yes	RISING	Clock trigger

Timing Diagram


Ramdsynr
AOUT
AIN
DIN
DOUT
WEN
OEN
CLK
T(AOUT)
XX
00
01
02
03
1C
1D
1E
1F
3
2
1
0
X
F
E
D
C
6u
6.5u
7u
Time (Seconds)

RAMS

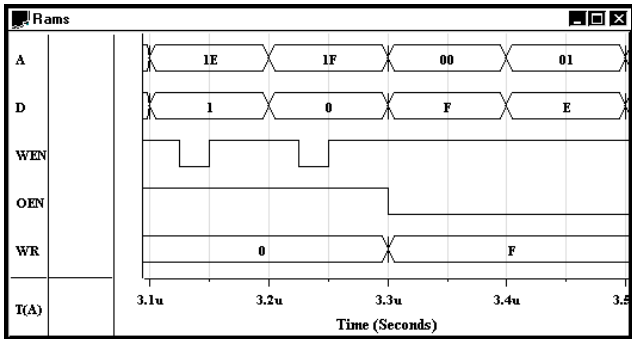
32 X 4 asynchronous single port RAM



Pins

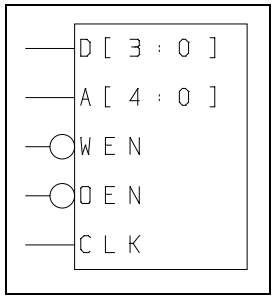
Pin	Description
A[4:0]	Read/Write address bus
D[3:0]	Bidirectional Data input/output bus
WEN	Active low write enable
OEN	Active low output enable

Timing Diagram



RAMSSYNC

32 X 4 synchronous single port RAM



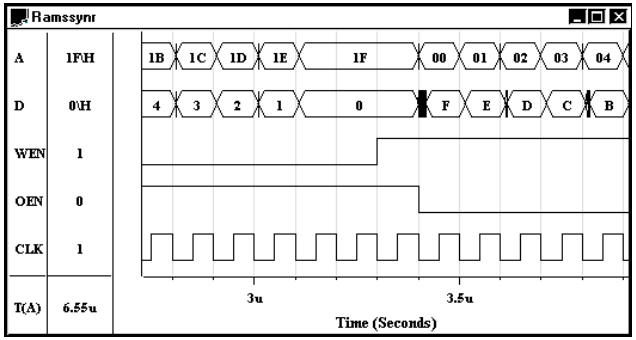
Pins

Pin	Description
A[4:0]	Read/Write address bus
D[3:0]	Bidirectional Data input/output bus
CLK	Clock
WEN	Active low write enable
OEN	Active low output enable

Attributes

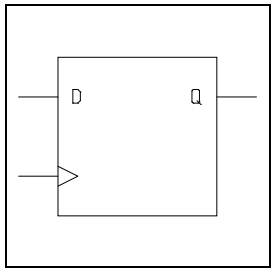
Attribute	Required	Default Value	Description
CLOCKEDGE	Yes	RISING	Clock trigger

Timing Diagram



FD

Register

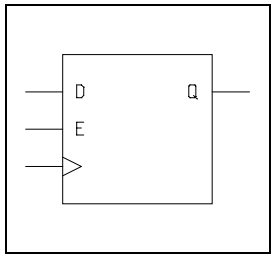


Truth Table

Input		Output
D	CLK	Q
x	0	q
d	r	d

FDE

Register with enable

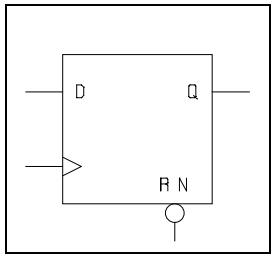


Truth Table

Input D	E	CLK	Output Q
x	0	x	q
x	1	0	q
d	1	r	d

FDRA

Register with reset

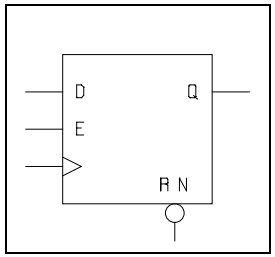


Truth Table

Input D	CLK	RN	Output Q
x	x	0	0
x	0	1	q
d	r	1	d

FDRAE

Register with reset enable

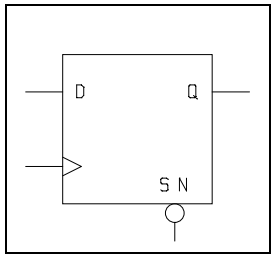


Truth Table

Input D	E	CLK	RN	Output Q
x	0	x	0	0
x	1	x	0	q
x	0	x	1	q
d	1	r	1	d

FDSA

Register with set

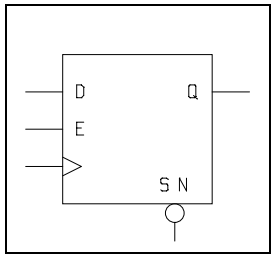


Truth Table

Input			Output
D	CLK	SN	Q
x	x	0	1
d	r	1	d

FDSAE

Register with set enable

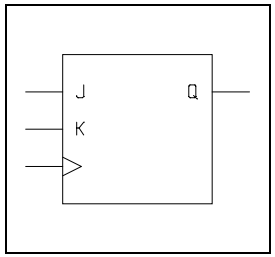


Truth Table

Input D	E	CLK	SN	Output Q
x	0	x	0	1
x	1	x	0	q
x	0	x	1	q
d	1	r	1	d

FJK

JK flip-flop

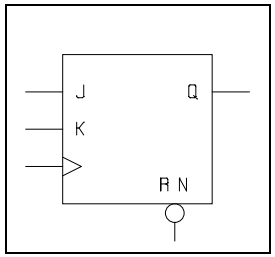


Truth Table

Input J	K	CLK	Output Q
x	x	0	q
0	0	r	q
1	0	r	1
0	1	r	0
1	1	r	q'

FJKRA

JK flip-flop with reset

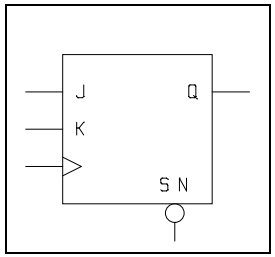


Truth Table

Input J	K	CLK	RN	Output Q
x	x	x	0	0
0	0	r	1	q
1	0	r	1	1
0	1	r	1	0
1	1	r	1	q'

FJKSA

JK flip-flop with set

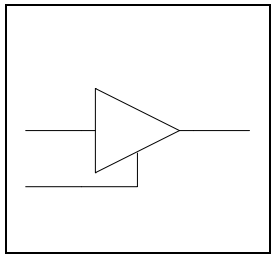


Truth Table

Input J	K	CLK	SN	Output Q
x	x	x	0	1
0	0	r	1	q
1	0	r	1	1
0	1	r	1	0
1	1	r	1	q'

BUFZ

Tri-state buffer

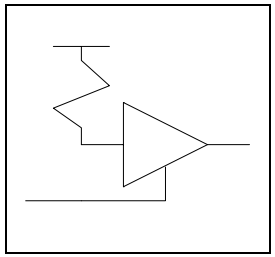


Truth Table

Input A	OE	Output Q
x	0	z
d	1	d

HZ

Tri-state high drive

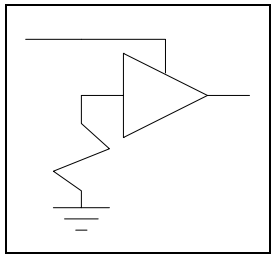


Truth Table

Input OE	Output Q
0	z
1	1

LZ

Tri-state low drive



Truth Table

Input OE	Output Q
0	z
1	0

Dynamic Macro Attributes

This section describes the dynamic macros for the AT40K. The macors are provided to give the user better control over the implementation of specific functions in a single core cell. It can also be used to simplify the design entry process. Pre-defined attributes with user designated values are used to exploit the logic capabilities of the AT40K core cell. The different pre-defined attributes that can be specified for the dynamic macros are listed below:

FUNCTIONG
FUNCTIONH
CLOCKEDGE
RSFUNCTION
RSPOLARITY
PRESERVE

Note: When dynamic macros are used in a design, the circuit cannot be simulated directly. It must be run through to *Initial Placement* before a functional netlist can be generated.

FUNCTIONG

Description

Specifies the equation to be implemented as the G output of the macro.

Value

An equation string of one to four variables. Details on the equation syntax are explained in the Equation Syntax section of this document.

FUNCTIONH

Description

Specifies the equation to be implemented as the H output of the macro.

Value

An equation string of one to four variables. Details on the equation syntax are explained in the Equation Syntax section of this document.

CLOCKEDGE

Description

Specifies the rising edge or falling edge trigger on the clock to which the register responds.

Value	Explanation
RISING	Positive edge trigger on the register CLK pin
FALLING	Negative edge trigger on the register CLK pin

RSFUNCTION

Description

The register in the AT40K core cell can provide set or reset functions through the RS pin on the dynamic macros.

Value	Explanation
RESET	RS functions as reset pin
SET	RS functions as set pin

RSPOLARITY

Description

Specifies the polarity of the RS pin.

Value	Explanation
HIGH	Active high RS pin
LOW	Active low RS pin

PRESERVE

Description

Specifies if the component should be preserved by the mapper during technology mapping.

Value	Explanation
YES	Don't touch the macro during mapping
NO	Macro can be flattened during mapping

Equation Syntax

The equation string attached to the FUNCTIONG and FUNCTIONH attributes describes the combinatorial behavior of the respective outputs of the core cell. To register and/or tri-state the output of the equation, the correct registered or tri-stated dynamic macros must be used from the library. The equation string is a multi-level sum-of-products equation built using the operators shown in the table below.

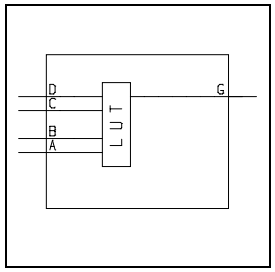
Operators	Description
^, ~	Logical NOT
*, &	Logical AND
|, +	Logical OR
#, @	Logical XOR

The dynamic macro input port names, called A, B, C, and D, are the variables used in the equation. Unconnected input ports are allowed on dynamic macro instances. However, an error will be generated if a port name used in the equation string is not connected to a net. The CLK, RS, and OE pins on the register and tri-state dynamic macros should not be used in the equation string.

The following section describes the dynamic macros available and the attributes required.

FGEN1

This is an *n* input function generator ($1 \leq n \leq 4$)



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
G	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

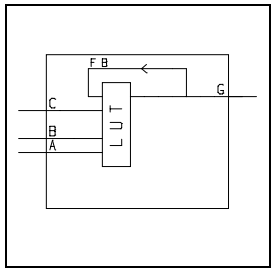
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
PRESERVE	No	NO	Mapping option

Example Function

FUNCTIONG = A * B * C * D

FGEN1F

This is an *n* input function generator with combinatorial feedback ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
G	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string

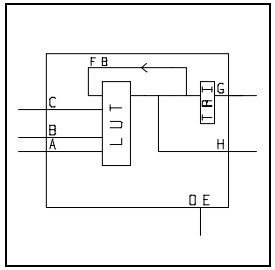
FB is the name of the combinatorial feedback signal.
The equation string for FUNCTIONG must contain the literal FB.

Example Function

FUNCTIONG = A & B & C & FB

FGEN1FT

This is an *n* input function generator with combinatorial feedback, followed by a tri-state buffer ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
OE	Tri-state enable
G	Tri-stated output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string

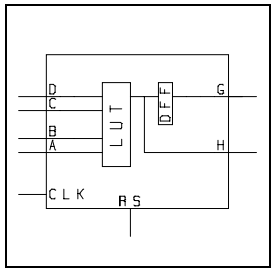
FB is the name of the combinatorial feedback signal.
The equation string for FUNCTIONG must contain the literal FB.

Example Function

FUNCTIONG = A & B & C + (~FB)

FGEN1R

This is an *n* input function generator followed by a register ($1 \leq n \leq 4$)



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
CLK	Clock
RS	Set or Reset
OE	Tri-state enable
G	Registered output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

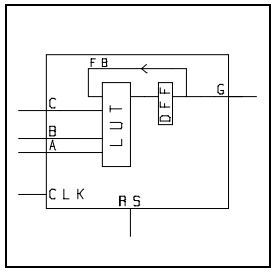
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin
PRESERVE	No	NO	Mapping option

Example Function

FUNCTIONG = (A + B + C) # D

FGEN1RF

This is an *n* input function generator with registered feedback ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
CLK	Clock
RS	Set or Reset
OE	Tri-state enable
G	Registered output of the function defined by FUNCTIONG attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

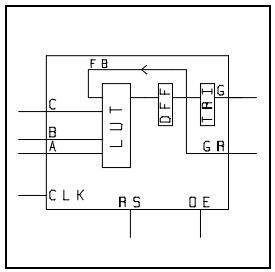
FB is the name of the combinatorial feedback signal.
The equation string for FUNCTIONG must contain the literal FB.

Example Function

FUNCTIONG = A & B & C & FB

FGEN1RFT

This is an *n* input function generator with registered feedback, followed by a tri-state buffer ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
CLK	Clock
RS	Set or Reset
OE	Tri-state enable
G	Registered, tri-stated output of the function defined by FUNCTIONG attribute
GR	Registered output of the function defined by FUNCTIONG attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

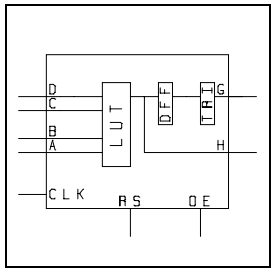
FB is the name of the combinatorial feedback signal.
The equation string for FUNCTIONG must contain the literal FB.

Example Function

FUNCTIONG = A * B * C * FB

FGEN1RT

This is an *n* input function generator followed by a register and tri-state buffer ($1 \leq n \leq 4$)



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
CLK	Clock
RS	Set or Reset
OE	Tri-state enable
G	Registered, tri-stated output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

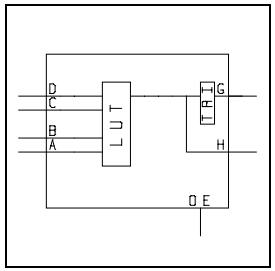
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin
PRESERVE	No	NO	Mapping option

Example Function

FUNCTIONG = A & B & C & (~D)

FGEN1T

This is an *n* input function generator followed by a tri-state buffer ($1 \leq n \leq 4$)



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
OE	Tri-state enable
G	Tri-stated output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONG attribute

Attributes

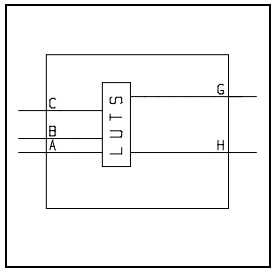
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
PRESERVE	No	NO	Mapping option

Example Function

FUNCTIONG = A # B # C # (~D)

FGEN2

This component has two *n* input function generators ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
G	Combinatorial output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

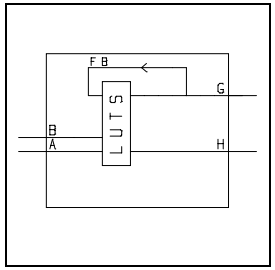
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

Example Function

FUNCTIONG = A * B * C
FUNCTIONH = A | B | C

FGEN2F

This component has two *n* input function generators with combinatorial feedback from G output ($1 \leq n \leq 2$)



Pins

Pin	Description
A	Input
B	Input
G	Combinatorial output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

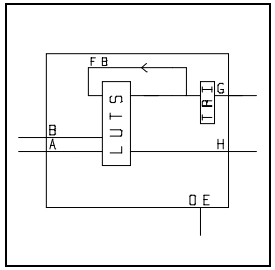
FB is the name of the combinatorial feedback signal from the G output.
The literal FB is required in the equation string for FUNCTIONG.
The literal FB is optional in the equation string for FUNCTIONH.

Example Function

FUNCTIONG = (B & FB) + (~B & FB)
FUNCTIONH = A + B

FGEN2FT

This component has two *n* input function generators with one output tri-stated and the other combinatorial ($1 \leq n \leq 2$)



Pins

Pin	Description
A	Input
B	Input
OE	Tri-state enable
G	Tri-stated output of the function defined by FUNCTIONG attribute using combinatorial feedback
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

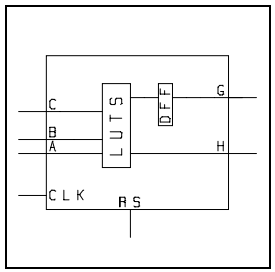
FB is the name of the combinatorial feedback signal from the G output.
The literal FB is required in the equation string for FUNCTIONG.
The literal FB is optional in the equation string for FUNCTIONH.

Example Function

FUNCTIONG = (A * B) # (B + FB)
FUNCTIONH = A # B

FGEN2R

This component has two *n* input function generators with one output registered and the other combinatorial ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
CLK	Clock
RS	Set or Reset
G	Registered output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

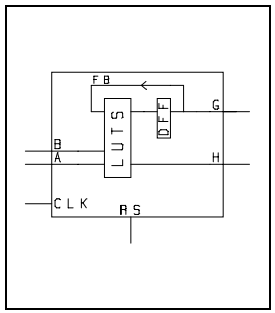
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

Example Function

FUNCTIONG = A * B * C
FUNCTIONH = A | B | C

FGEN2RF

This component has two *n* input function generators with one output registered and the other combinatorial ($1 \leq n \leq 2$)



Pins

Pin	Description
A	Input
B	Input
OE	Tri-state enable
CLK	Clock
RS	Set or Reset
G	Registered output of the function defined by FUNCTIONG attribute using registered feedback
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

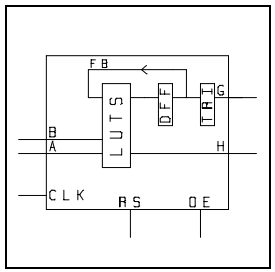
FB is the name of the registered feedback signal from the G output.
The literal FB is required in the equation string for FUNCTIONG.
The literal FB is optional in the equation string for FUNCTIONH.

Example Function

FUNCTIONG = (A * B) # (B + FB)
FUNCTIONH = A # B

FGEN2RFT

Two *n* input function generators with one output registered, tri-stated and the other combinatorial ($1 \leq n \leq 2$)



Pins

Pin	Description
A	Input
B	Input
OE	Tri-state enable
CLK	Clock
RS	Set or Reset
G	Registered output of the function defined by FUNCTIONG attribute using registered feedback
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

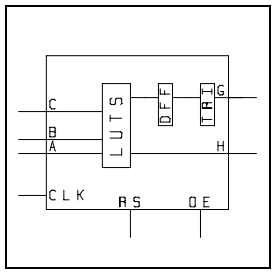
FB is the name of the registered feedback signal from the G output.
The literal FB is required in the equation string for FUNCTIONG.
The literal FB is optional in the equation string for FUNCTIONH.

Example Function

```
FUNCTIONG = (A * B ) # (B * FB)
FUNCTIONH = A # B
```

FGEN2RT

Two *n* input function generators with one output registered, tri-stated and the other combinatorial ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
OE	Tri-state enable
CLK	Clock
RS	Set or Reset
G	Registered, tri-stated output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

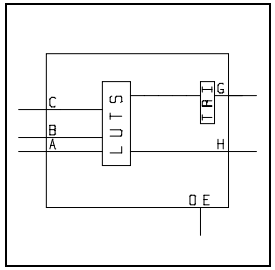
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

Example Function

FUNCTIONG = A * B * C
FUNCTIONH = A # B # C

FGEN2T

Two *n* input function generators with one output tri-stated and the other combinatorial ($1 \leq n \leq 3$)



Pins

Pin	Description
A	Input
B	Input
C	Input
OE	Tri-state enable
G	Tri-stated output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

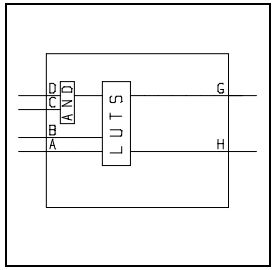
Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

Example Function

FUNCTIONG = A * B * C
FUNCTIONH = A # B # C

MGEN

Two 3-input function generators. This is a special case macro (typically used in multipliers) with an upstream AND gate feeding the Look Up Tables.



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
G	Combinatorial output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

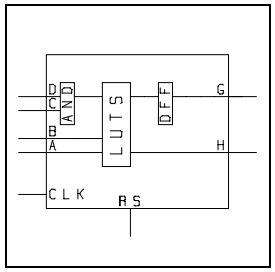
FUNCTIONG and FUNCTIONH must have the expression (C*D) in the equation string, as the upstream AND gate is connected to pins C and D.

Example Function

FUNCTIONG = A # B # (C*D)
FUNCTIONH = (C*D)*A + (C*D)*B + A*B

MGENR

Two 3-input function generators with one output registered and the other combinatorial. This is a special case macro (typically used in pipelined multipliers) with an upstream AND gate feeding the Look Up Tables.



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
CLK	Clock
RS	Set or Reset
G	Registered output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

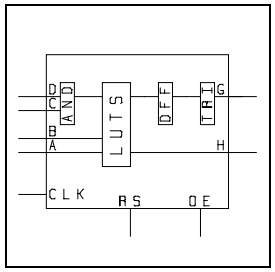
FUNCTIONG and FUNCTIONH must have the expression (C*D) in the equation string, as the upstream AND gate is connected to pins C and D.

Example Function

```
FUNCTIONG = A * B * (C*D)
FUNCTIONH = (C*D)*A + (C*D)*B + A*B
```

MGENRT

Two 3-input function generators with one output registered, tri-stated, and the other combinatorial. This is a special case macro (typically used in pipelined multipliers) with an upstream AND gate feeding the Look Up Tables.



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
CLK	Clock
RS	Set or Reset
OE	Tri-state enable
G	Registered output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string
CLOCKEDGE	Yes	RISING	Clock trigger
RSFUNCTION	Yes	RESET	RS pin functionality
RSPOLARITY	Yes	LOW	Active polarity of RS pin

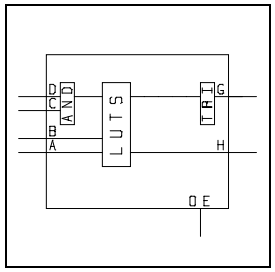
FUNCTIONG and FUNCTIONH must have the expression (C*D) in the equation string, as the upstream AND gate is connected to pins C and D.

Example Function

FUNCTIONG = A * B * (C*D)
FUNCTIONH = (C*D)*A + (C*D)*B + A*B

MGENT

Two 3-input function generators with one output tri-stated and the other combinatorial. This is a special case macro (typically used in multipliers) with an upstream AND gate feeding the Look Up Tables.



Pins

Pin	Description
A	Input
B	Input
C	Input
D	Input
OE	Tri-state enable
G	Registered output of the function defined by FUNCTIONG attribute
H	Combinatorial output of the function defined by FUNCTIONH attribute

Attributes

Attribute	Required	Default Value	Description
FUNCTIONG	Yes	?	Equation string
FUNCTIONH	Yes	?	Equation string

FUNCTIONG and FUNCTIONH must have the expression (C*D) in the equation string, as the upstream AND gate is connected to pins C and D.

Example Function

FUNCTIONG = A * B * (C*D)
FUNCTIONH = (C*D)*A + (C*D)*B + A*B