Programming Specification for AT17LV(A) Series FPGA Configuration Memories

The FPGA Configurator

The FPGA Configurator is a serial EEPROM memory that can also be used to load programmable devices. This document describes the features needed to program the Configurator from within its programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low[1]).

Note: 1. The $\overline{\text{SER\_EN}}$ pin must be driven low if the programming mode is used immediately after power-up.

There are many ways to program an AT17LV(A) Series Configurator:

- Using a third-party programmer
- Using Atmel's Configurator Programming Kit ATDH2200E
- Using Atmel's Configurator Programming Cable ATDH2225
- Using a custom programming solution

For details of other programming options, please refer to "Introducing Atmel Configurators" application note, available on the Atmel web site (www.atmel.com).

Serial Bus Overview

The serial bus is a 2-wire bus. One wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a Start Condition and is ended with a Stop Condition. The message consists of an integer number of bytes, each byte consisting of 8 bits of data, followed by a 9th Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted byte. This is possible because devices may only drive the DATA line Low. The system must provide a small pull-up current for the DATA line.

The MESSAGE FORMAT for read and write instructions consists of the bytes shown in "Bit Format" on page 2.

While writing, the programmer is responsible for issuing the instruction and data. While reading, the programmer issues the instruction and acknowledges the data from the Configurator as necessary.

Again, the Acknowledge Bit is asserted on the DATA line by the receiving device on a byte-by-byte basis.

The factory blanks devices to all zeros before shipping. The array cannot otherwise be "initialized" except by explicitly writing a known value to each location using the serial protocol described herein.

AT17LV(A) Series FPGA Configuration Memory

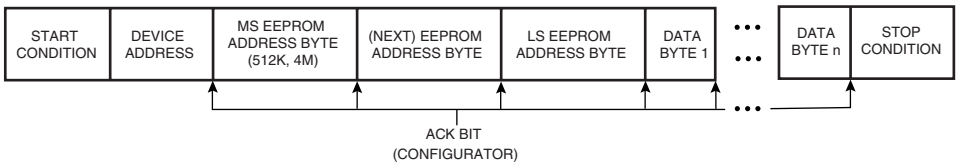
Application Note

Rev. 0437K–CNFG–05/03

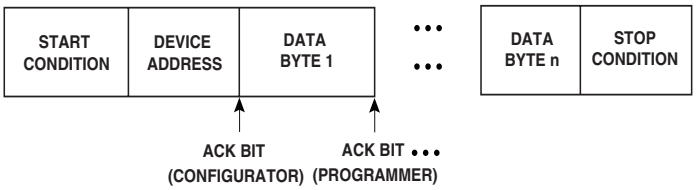
Bit Format

Data on the DATA pin may change only during the CLOCK Low time; whereas Start and Stop Conditions are identified as transitions during the CLOCK High time.

Write Instruction Message Format



Current Address Read (Extended to Sequential Read) Instruction Message Format



Start and Stop Conditions

The Start Condition is indicated by a high-to-low transition of the DATA line when the CLOCK line is High. Similarly, the Stop Condition is generated by a low-to-high transition of the DATA line when the CLOCK line is High, see Figure 1.

The Start Condition will return the device to the state where it is waiting for a Device Address (its normal quiescent mode).

The Stop Condition initiates an internally timed write signal whose maximum duration is t_{WR} (refer to the AC Characteristics tables for actual value). During this time, the Configurator must remain in programming mode (i.e., $\overline{\text{SER\_EN}}$ is driven Low). DATA and CLOCK lines are ignored until the cycle is completed. Since the write cycle typically completes in less than t_{WR} seconds, we recommend the use of “polling” as described in page 8. Input levels to all other pins should be held constant until the write cycle has been completed.

Acknowledge Bit

The Acknowledge (ACK) Bit shown in Figure 1 is provided by the Configurator receiving the byte. The receiving Configurator can accept the byte by asserting a Low value on the DATA line, or it can refuse the byte by asserting (allowing the signal to be externally pulled up to) a High value on the DATA line. All bytes from accepted messages must be terminated by either an Acknowledge Bit or a Stop Condition. Following an ACK Bit, when the DATA line is released during an exchange of control between the Configurator and the Programmer, the DATA line may be pulled High temporarily as shown above due to the open-collector output nature of the line. Control of the line must resume before the next rising edge of the clock.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on the DATA line for the Device Address Byte and the EEPROM Address Bytes. It is followed by the lesser significant bits until the eighth bit, the least significant bit, is transmitted. However, for Data Bytes (both writing and reading), the first bit transmitted is the least significant bit. This protocol is shown in "Device Address Byte" and "EEPROM Address".

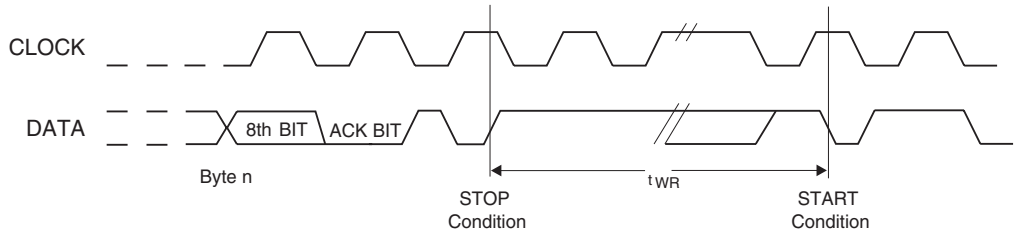
Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A2 bit is provided to allow multiple Configurators to share a common bus. When programming a Configurator, the A2 pin on the Configurator must be forced to a logic "0" or "1" level. It is recommended that this pin be connected to 0V (GND) using a 4.7 kΩ pull-down resistor – thereby matching the default setting of Atmel's AT17 Configurator Programming System (CPS). Thus, the A2[1] bit may be used as an Address Bit among two Configurators, or as a chip-enable mechanism for in-system programming employing more than two Configurators.

Note: 1. Configurators that have a B label on the date code; only the A2 input pin will be pulled to ground via weak internal pull-downs if left floating.

The $\overline{CE}$ pin cannot be used for device selection in programming mode (i.e., when $\overline{SER\_EN}$ is drive Low).

Figure 1. Start and Stop Conditions



Device Address Byte

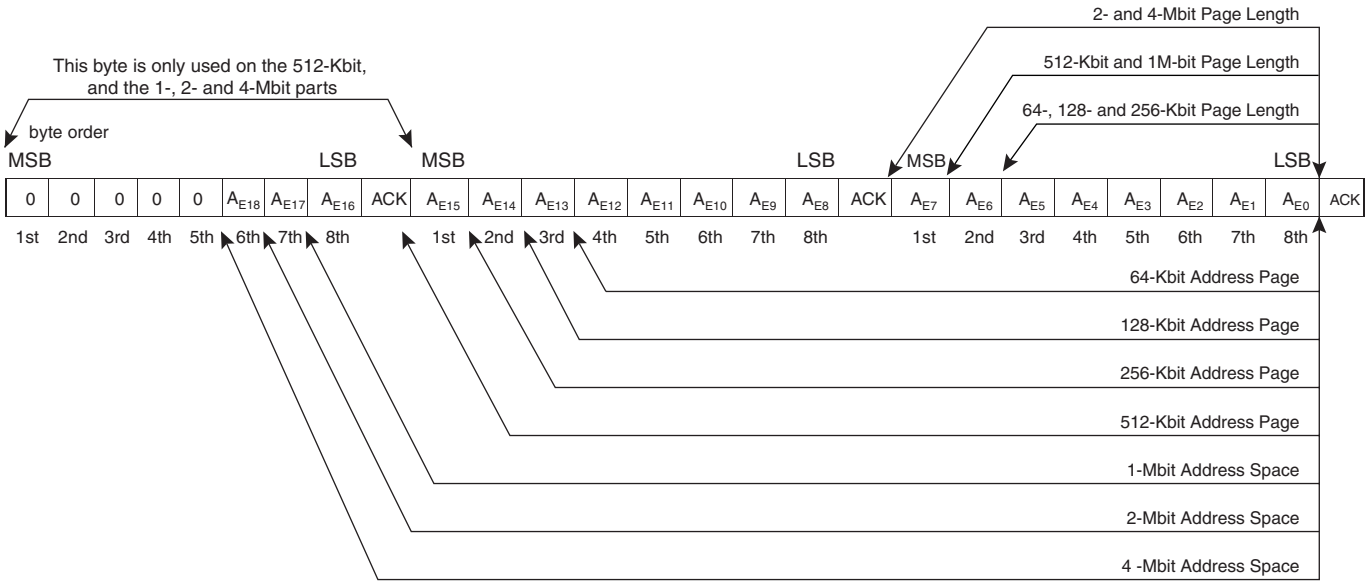
MSB							LSB
1	0	1	0	A_2	1	1	R/$\overline{W}$
1st	2nd	3rd	4th	5th	6th	7th	8th

Where: R/$\overline{W}$ = 1 Read
= 0 Write
A2 = 1 if A2 pin of target Configurator is at V_{CC}
= 0 if A2 pin of target Configurator is at GROUND

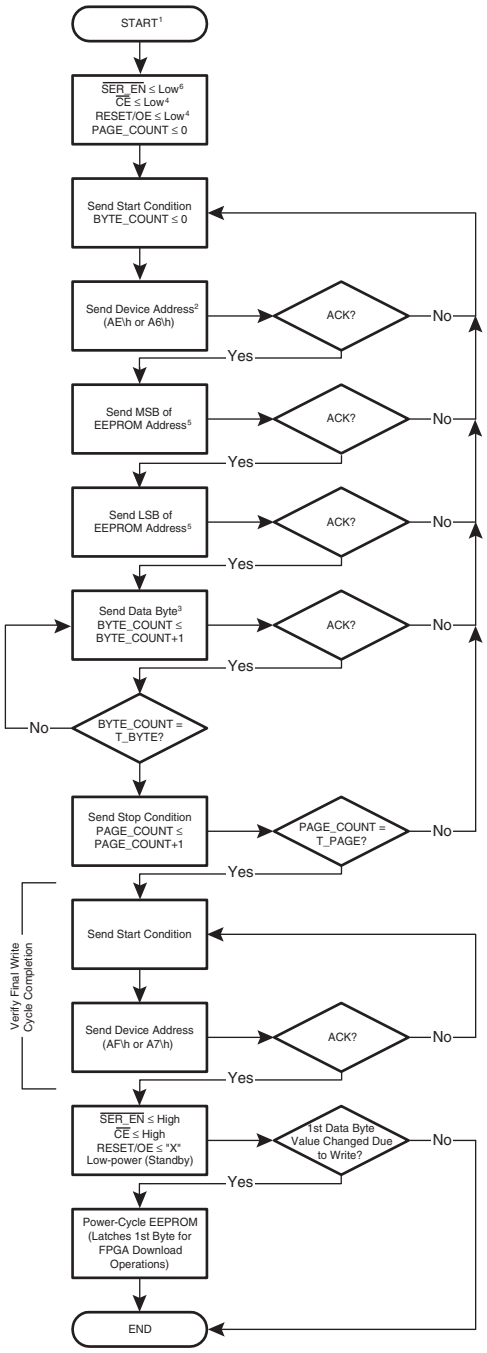
EEPROM Address

The EEPROM Address consists of two bytes on the 64-, 128- and 256-Kbit parts, and three bytes on the 512-Kbit, 1- and 2- and 4-Mbit parts. Each Address Byte is followed by an Acknowledge Bit (provided by the Configurator). These bytes define the normal address space of the Configurator, as described below. The order in which each byte is clocked into the Configurator is also indicated. Unused bits in an Address Byte must be set to “0”. Exceptions to this are:

- when setting the reset polarity;
- when reading Device and Manufacturer Codes; and
- when enabling/disabling the internal oscillator in the AT17A Series Configurator (512-Kbit, 1-, 2- and 4-Mbit parts only).



Programming Summary: Write to Whole Device



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$), which depends on the A2 bit setting
3. Data byte received/sent LSB to MSB
4. These signals have "don't care" conditions for the AT17LV512(A)/010(A)/002(A) and AT17LV040.
5. The 512-Kbit, and 1-, 2- and 4-Mbit parts require three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.
6. WP pins on 512-Kbit, and 1- and 2-Mbit devices are internally pulled to GND; by default disabling the write protect feature of the devices.

EEPROM Address is Defined as:

65(A)			$000x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
128(A)			$00x_7x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
256(A)			$0x_8x_7x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
512(A)	0000	0000	$x_8x_7x_6x_5$	$x_4x_3x_2x_1$	x_0000	0000
010(A)	0000	$000x_9$	$x_8x_7x_6x_5$	$x_4x_3x_2x_1$	x_0000	0000
002(A)	0000	$00x_{9X8}$	$x_7x_6x_5x_4$	$x_3x_2x_1x_0$	0000	0000
040	000	$0x_{10X9X8}$	$x_7x_6x_5x_4$	$x_3x_2x_1x_0$	0000	0000

Note: 1. where X_n ... X_0 is (PAGE_COUNT)\b
where X_n ... X_0 is (PAGE_COUNT)\b

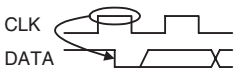
T_BYTE Per Page

AT17LV65(A)/128(A)/256(A)	64
AT17LV512(A)/010(A)	128
AT17LV002(A)	256
AT17LV040	256

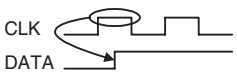
T_PAGE

AT17LV65(A)	128
AT17LV128(A)	256
AT17LV256(A)	512
AT17LV512(A)	512
AT17LV010(A)	1024
AT17LV002(A)	1024
AT17LV040	2048

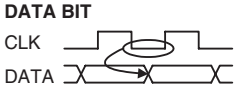
START CONDITION



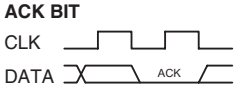
STOP CONDITION



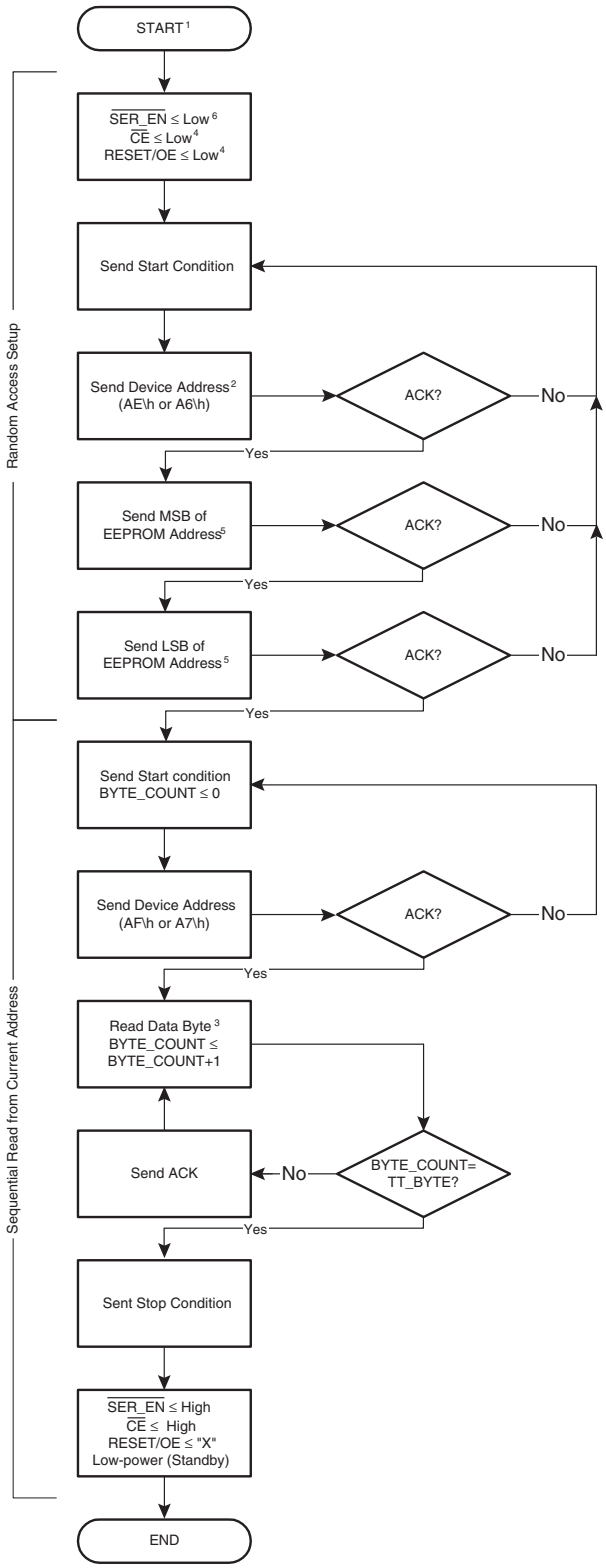
DATA BIT



ACK BIT



Programming Summary: Read from Whole Device



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$)
3. Data byte received/sent LSB to MSB
4. These signals have "don't care" conditions for the AT17LV512(A)/010(A)/002(A) and AT17LV040.
5. The 512-Kbit, and 1-, 2- and 4-Mbit parts require three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.
6. WP pins on 512-Kbit, and 1-, 2- and 4-Mbit devices are internally pulled to GND; by default disabling the write protect feature of the devices.

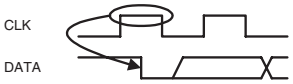
EEPROM Address is Defined as:

65(A)/128(A)/256(A)	00 00 \h
512(A)/010(A)/002(A) and 040	00 00 00 \h

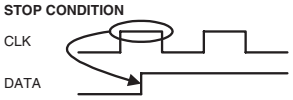
TT_BYTE

AT17LV65(A)	8192 \d
AT17LV128(A)	16384 \d
AT17LV256(A)	32768 \d
AT17LV512(A)	65536 \d
AT17LV010(A)	131072 \d
AT17LV002(A)	262144 \d
AT17LV040	524288 \d

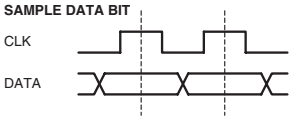
START CONDITION



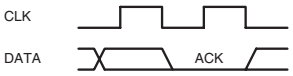
STOP CONDITION



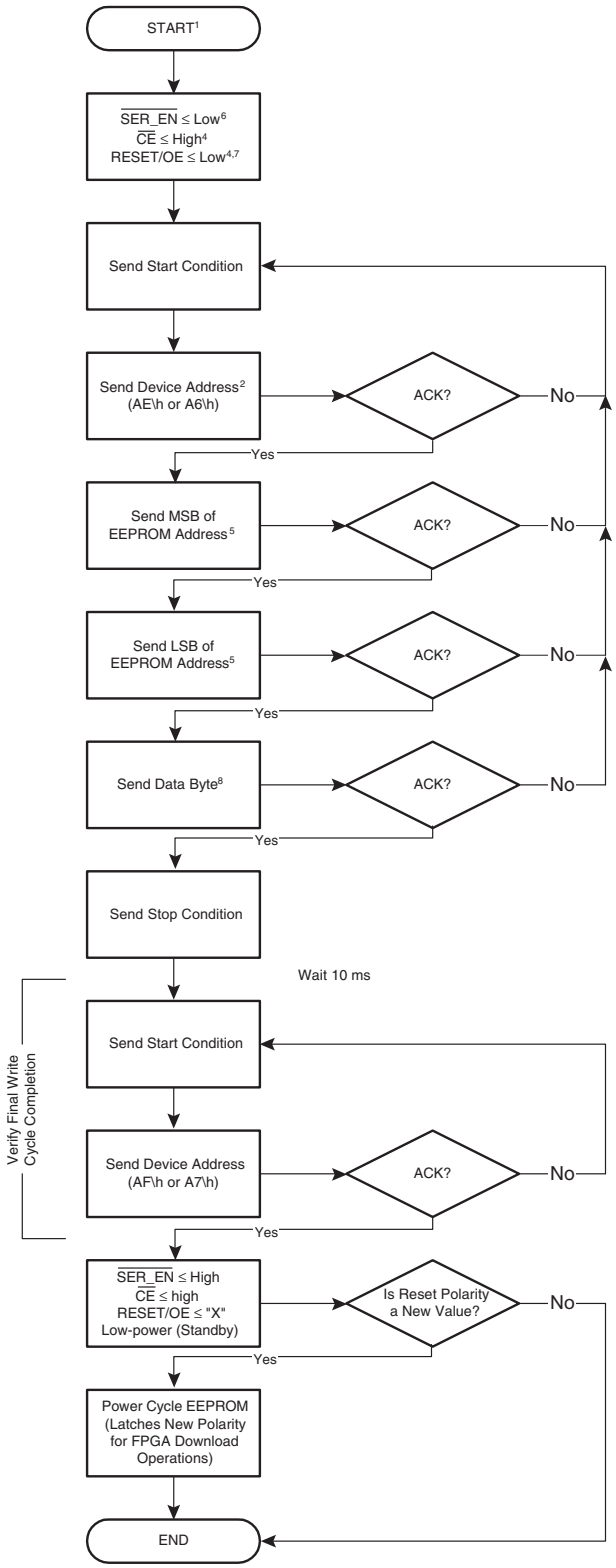
SAMPLE DATA BIT



ACK BIT



Programming Summary: Write Reset Polarity



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$)
3. Data byte received/sent LSB to MSB
4. These signals have "don't care" conditions for the AT17LV512(A)/010(A)/002(A) and AT17LV040.
5. The 512-Kbit, and 1-, 2- and 4-Mbit parts require three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.
6. WP pins on 512-Kbit, and 1-, 2- and 4-Mbit devices are internally pulled to GND; by default disabling the write protect feature of the devices.
7. Drive RESET/OE high for active low RESET, active high OE. Drive RESET/OE low for active high RESET, active low OE.
8. The 512-Kbit, and 1-, 2- and 4-Mbit parts require four data bytes of the same value to program the reset polarity; all four bytes must be individually ACK'd by the EEPROM.

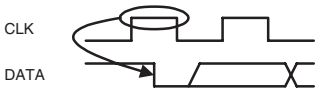
EEPROM Address is Defined as:

AT17LV65(A)/128(A)/256(A)	3F FF \h
AT17LV512(A)/010(A)	02 00 00 \h
AT17LV002(A)	400 000 \h
AT17LV040	400 000 \h

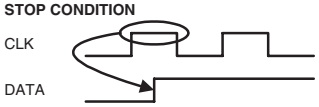
Data Byte is Defined as:

65(A)/128(A)/256(A)	FF \h
512(A)/010(A)/002(A) and 040 (active low RESET)	FF \h
512(A)/010(A)/002(A) and 040 (active high RESET)	00 \h

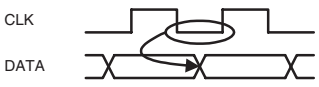
START CONDITION



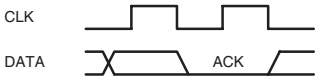
STOP CONDITION



DATA BIT



ACK BIT



Data Byte

The organization of the Data Byte is shown below. Note that in this case, the Data Byte is clocked into the device LSB first and MSB last.

Writing

Writing to the normal address space takes place in pages. A page is 64 bytes long in 64-, 128-, and 256-Kbit parts; 128 bytes long in 512-Kbit and 1-Mbit parts, and 256 bytes long in the 2- and 4-Mbit parts. The page boundaries are, respectively, addresses where A_{E6} down to A_{EOS} are all zero, and A_{E6} down to A_{E0} are all zero. Writing can start at any address within a page and the number of bytes written must be 64 for the 64-, 128- and 256-Kbit parts, 128 for the 512-Kbit and 1-Mbit parts, and 256 for the 2- and 4-Mbit parts. The first byte is written at the transmitted address. The address is incremented in the Configurator following the receipt of each Data Byte. Only the lower bits of the address (6, 7 or 8, depending on the page length) are incremented. Thus, after writing to the last byte address within the given page, the address will roll over to the first byte address of the same page.

Data Byte

LSB MSB

D0	D1	D2	D3	D4	D5	D6	D7
1st	2nd	3rd	4th	5th	6th	7th	8th

```
A Write Instruction consists of
    a Start Condition
    a Device Address Byte with R/W = 0
      An Acknowledge Bit from the Configurator
    MS Byte of the EEPROM Address (512-Kbit, and 1-, 2- and 4-Mbit parts only)
      An Acknowledge Bit from the Configurator
    (Next) Byte of the EEPROM Address
      An Acknowledge Bit from the Configurator
    LS Byte of EEPROM Address
      An Acknowledge Bit from the Configurator
    One or more Data Bytes (sent to the Configurator)
      Each followed by an Acknowledge Bit from the Configurator
    a Stop Condition
```

WRITE POLLING: On receipt of the Stop Condition, the Configurator enters an internally-timed write cycle. While the Configurator is busy with this write cycle, it will not acknowledge any transfers. The programmer can start the next page write by sending the Start Condition followed by the Device Address, in effect polling the Configurator. If this is not acknowledged, then the programmer should abandon the transfer without asserting a Stop Condition. The programmer can then repeatedly initiate a write instruction as above, until an acknowledge is received. When the Acknowledge Bit is received, the write instruction should continue by sending the first EEPROM Address Byte to the Configurator.

An alternative to write polling would be to wait a period of t_{WR} before sending the next page of data or exiting the programming mode. All signals must be maintained during the entire write cycle.

Reading

Read instructions are initiated similarly to write instructions, but the R/$\overline{W}$ bit in the Device Address is set to one. There are three variants of the read instruction: current address read, random read and sequential read.

For all reads, it is important to understand that the internal Data Byte address counter maintains the last address accessed during the previous read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode (i.e., $\overline{SER\_EN}$ is driven Low). If the last operation was a read at address *n*, then the current address would be *n* + 1. If the final operation was a write at address *n*, then the current address would again be *n* + 1 with one exception. If address *n* was the last byte address in the page, the incremented address *n* + 1 would "roll over" to the first byte address on the next page.

CURRENT ADDRESS READ: Once the Device Address (with the R/$\overline{W}$ select bit set to High) is clocked in and acknowledged by the Configurator, the Data Byte at the current address is serially clocked out by the Configurator in response to the clock from the programmer. The programmer generates a Stop Condition to accept the single byte of data and terminate the read instruction.

```
A Current Address Read instruction consists of
    a Start Condition
    a Device Address with R/W = 1
      An Acknowledge Bit from the Configurator
    a Data Byte from the Configurator
    a Stop Condition from the programmer.
```

RANDOM READ: A Random Read is a Current Address Read preceded by an aborted write instruction. The write instruction is only initiated for the purpose of loading the EEPROM Address Bytes. Once the Device Address Byte and the EEPROM Address Bytes are clocked in and acknowledged by the Configurator, the programmer immediately initiates a Current Address Read.

```
A Random Address Read instruction consists of
  a Start Condition
  a Device Address with R/W = 0
    An Acknowledge Bit from the Configurator
  MS Byte of the EEPROM Address (512-Kbit, and 1-, 2- and 4-Mbit parts only)
    An Acknowledge Bit from the Configurator
  (Next) Byte of the EEPROM Address
    An Acknowledge Bit from the Configurator
  LS Byte of EEPROM Address
    An Acknowledge bit from the Configurator
  a Start Condition
  a Device Address with R/W = 1
    An Acknowledge Bit from the Configurator
  a Data Byte from the Configurator
  a Stop Condition from the programmer.
```

SEQUENTIAL READ: Sequential Reads follow either a Current Address Read or a Random Address Read. After the programmer receives a Data Byte, it may respond with an Acknowledge Bit. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached. The Sequential Read instruction is terminated when the programmer does not respond with an Acknowledge Bit, but instead generates a Stop Condition following the receipt of a Data Byte.

Programmer Functions

The following programmer functions are supported while the Configurator is in programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low):

1. Reading the Manufacturer's Code and the Device Code, optional for in-system programming (ISP).
2. Programing the device.
3. Verifying the device.
4. Setting the Reset Polarity option.
5. Enabling/disabling the internal oscillator.

In the order given above, they are performed in the following manner. The same protocol and operations are used for both 5V and 3.3V devices, as well as for the Altera pinout variants except where stated.

Reading Manufacturer's and Device Codes

The 512(A)/010(A) Configurators use a different algorithm than the 65(A)/128(A)/256(A) Configurators, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 040000H.

On 002(A)/040 Configurators, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 100000H.

On 65(A)/128(A)/256(A) Configurators, the sequential read is done at EEPROM Address 0 by performing a Current Address Read with the following additional DC voltages set:

```
RESET/OE      = 0V
CE            = 11.5 ± 0.5V
```

The correct codes are[1]:

Manufacturers Code - Byte 0		1E	All
Device Code	- Byte 1	FF	AT17LV128(A)
		7F	AT17LV65(A)
		77	AT17LV256(A)
		37	AT17LV512(A)
		F7	AT17LV010(A)
		78	AT17LV002(A)
		74	AT17LV040

Note: 1. The Manufacturer's Code and Device Code are read using the byte ordering specified for Data Bytes; i.e., LSB first, MSB last. These procedures are not supported by the supplied ISP reference design schematics for 65(A)/128(A)/256(A) Configurators. After reading the manufacturer identification bytes, a hardware power cycle (power on reset) is required in order to access the actual location of the memory in the programming mode. For the new devices (35.5 process), toggling the $\overline{\text{SER\_EN}}$ pin from Low to High and the Low with respect to the programming clock cycle will automatically exit the manufacturer identification read mode without power cycle.

Programming the Device

All the bytes in a given page must be written. The page access order is not important but it is suggested that the Configurator be written sequentially from address 0. Writing is accomplished by using the DATA and CLOCK pins.

For the 65(A)/128(A)/256(A) Configurators only, two additional programming pins must be set as follows:

```
RESET/OE (OE)= 0V (Write protection disable)
CE (nCS)     = 0V
```

Important Note on AT17LV(A) and AT17A Series Configurators Programming

The first byte of data will not be cached for read back during FPGA Configuration (i.e., when $\overline{\text{SER\_EN}}$ is driven High) until the Configurator is power-cycled. This may be critical in cascaded ISP applications where the first byte of the second or subsequent EEPROM is likely to change between updated bitstreams.

Write Protect Operation

The AT17LV(A) Series Configurators have a "Write Protect" feature that allows portions of the memory to be blocked during Write instructions. When the blocking is in effect, data will not be written in the blocked portion and the existing data in the blocked portion will be preserved.

For the 65(A)/128(A)/256(A) Configurators, the RESET/$\overline{\text{OE}}$ ($\overline{\text{OE}}$) pin is used as a WRITE PROTECT pin while in programming mode (i.e., $\overline{\text{SER\_EN}}$ is Low with $\overline{\text{CE}}$ (nCS) Low). When the RESET/$\overline{\text{OE}}$ ($\overline{\text{OE}}$) pin is High under these conditions, memory is protected as follows:

65: The lower 1/2 of memory is protected
(address 0000 - 0FFF)

128: The lower 1/4 of memory is protected
(address 0000 - 0FFF)

256: The lower 1/4 of memory is protected
(address 0000 - 1FFF)

For the Configurators, there are up to two dedicated Write Protect[1] pins: WP1 and WP2. They are decoded to provide protection as described below. (WP1/WP2 have weak internal pull-downs by default.)

Note: 1. The AT17512A/010A/002A parts do not support WP2. The AT17LV040 Configurator does not have Write Protect pins.

AT17LV512/010 Write Protection

WP2	WP1	Protection
0	0	No protection
0	1	Addresses 00000 - 07FFF (1/4 of 010, 1/2 of 512)
1	0	Addresses 00000 - 0FFFF (1/2 of 010, All of 512)
1	1	Addresses 00000 - 17FFF (3/4 of 010, All of 512)

AT17LV512A/010A Write Protection

WP1	Protection
0	No protection
1	Addresses 00000 - 07FFF (1/4 of 010A, 1/2 of 512A)

AT17LV002 Series Write Protection

WP2	WP1	Protection
0	0	No protection/Normal mode
0	1	Addresses 0X000000 - 0X00FFFF (1/4 of 002)
1	0	Addresses 0X000000 - 0X01FFFF (1/2 of 002)
1	1	Addresses 0X000000 - 0X02FFFF (3/4 of 002)

AT17LV002A Series Write Protection

WP1	Protection
0	No protection
1	Addresses 0X000000 - 0X00FFFF (1/4 of 002A)

There is no physical write protect pins for AT17LV040 configurators. However, the write protect feature for the AT17LV040 configurator can be determined by the state of two fuses through the 2-wire bus (Clock and Data) in the programming mode ($\overline{\text{SER\_EN}}$ is driven Low). The table below details the relationship between the level of protection and the state of each fuse.

AT17LV040 Series Write Protection

Fuse 1	Fuse 0	Protection
0	0	No protection/Normal mode
0	1	Addresses 0X000000 - 0X01FFFF (1/4 of 040)
1	0	Addresses 0X000000 - 0X03FFFF (1/2 of 040)
1	1	Addresses 0X000000 - 00X05FFFF (3/4 of 040)

To program the state of the fuses, set addresses <23:16> to 0010 0XXX and enter 4 bytes of data (0x0/0x1/0x2/0x3 for no 1/4, 1/2 or 3/4 protection - note that data is sent in LSB first) using the two-wire algorithm.

To read the state of the fuses, set addresses <23:16> to 0010 0XXX or 0011 0XXX (to read fuse 0 or 1, respectively) and use the random read algorithm. If the data is “FF FF FF FF”, the fuse is set High; if the data is “00 00 00 00”, the fuse is set to Low.

Verifying the Device

All bytes in the Configurator should be read and compared to their intended values. Reading is done using the CLOCK and DATA pins.

For the 65(A)/128(A)/256(A) Configurators, two additional programming pins must be set as follows:

RESET/$\overline{\text{OE}}$ ($\overline{\text{OE}}$)= 0V (Write protection disable)

$\overline{\text{CE}}$ (nCS) = 0V

RESET Polarity Option

All Configurators in the AT17LV(A) Series have the ability to change the polarity of the RESET/$\overline{\text{OE}}$ pin. This is required to allow the devices to properly configure various FPGA families. The default condition is active Low OE and active High RESET.

The 65(A)/128(A)/256(A) Configurators use a different algorithm from the 512(A)/010(A)/002(A) Configurators; the algorithms are described below.

65(A)/128(A)/256(A) Configurator RESET/$\overline{\text{OE}}$ Polarity Programming

Setting the polarity option active High OE (active Low RESET): Write Data Byte “FF” to address 3FFFH, with two additional programming pins set to the following:

RESET/$\overline{\text{OE}}$ ($\overline{\text{OE}}$)= V_{CC} +/- 0.25V

$\overline{\text{CE}}$ (nCS) = V_{CC} +/- 0.25V

Setting the polarity option active Low OE (active High RESET): Write a byte “FF” to address 3FFFH, with two additional programming pins set to the following:

RESET/$\overline{\text{OE}}$ ($\overline{\text{OE}}$)= 0V

$\overline{\text{CE}}$ (nCS) = V_{CC} +/- 0.25V

Verifying the RESET Polarity: Power up the device with:

RESET/$\overline{OE}$ ($\overline{OE}$) = 0V

$\overline{CE}$ (nCS) = 0V

A2/$\overline{CEO}$(A2/nCSA) = Input to programmer (High Z)

$\overline{SER\_EN}$ = V_{CC} +/- 0.25V

CLK (DCLK) = 0V

DATA = Input to programmer

In this condition, if the DATA pin is tri-stated, then the RESET/$\overline{OE}$ ($\overline{OE}$) fuse is programmed for active High OE (active Low RESET); if the DATA pin reads a “0” or a “1”, the RESET/$\overline{OE}$ ($\overline{OE}$) fuse is active Low OE (active High RESET).

512(A)/010(A) Configurator RESET/$\overline{OE}$ ($\overline{OE}$) Polarity Programming

Setting the polarity option active High OE (active Low RESET): Write four bytes “FF FF FF FF” to addresses 20000H - 20003H.

Setting the polarity option active Low OE (active High RESET): Write four bytes “00 00 00 00” to addresses 20000H - 20003H.

Verifying the RESET/$\overline{OE}$ Polarity 512(A)/010(A) Configurators: Perform a Random Read of four Data Bytes from addresses 20000H - 20003H. If the data is “00 00 00 00” then the fuse is programmed for active Low OE (active High RESET); if the data is “FF FF FF FF” then the fuse is programmed for active High OE (active Low RESET).

002(A)/040 Configurator RESET/$\overline{OE}$ Polarity Programming

Setting the polarity option active High OE (active Low RESET): Write four bytes “FF FF FF FF” to addresses 400000H - 400003H.

Setting the polarity option active Low OE (active High RESET): Write four bytes “00 00 00 00” to addresses 400000H - 400003H.

Verifying the RESET/$\overline{OE}$ Polarity 002(A)/040 Configurators: Perform a Random Read of four Data Bytes from addresses 400000H - 400003H. If the data is “00 00 00 00” then the fuse is programmed for active Low OE (active High RESET); if the data is “FF FF FF FF” then the fuse ISP programmed for active High OE (ACTIVE LOW RESET).

Important Notes on AT17LV(A) Series Configurators RESET Polarity Programming

1. The pin conditions above must be maintained during the entire write cycle; t_{WR} or until the next Device Address is acknowledged (if using Write polling).
2. After the RESET polarity has been modified, the Configurator must be powered down and back up again before attempting to verify functionality or use the newly programmed RESET function.

DCLK Pin Option

The AT17LV512A/010A/002A devices have the ability to disable their DCLK output. These devices can be used in Master mode where the clock pin is an output, or in Slave mode where the clock pin is an input.

The mode is normally determined by the state of the nCS pin on power-up and reset. However, there are instances where it may be desirable to program the device into Slave mode regardless of the power-up sequence.

The default status of the DCLK pin is with the internal oscillator enabled.

To disable the internal oscillator and program the device into Slave mode for the 512A/010A:

Write a byte “00” of data to Address 38XXXXH with nCS held to ground.

To disable the internal oscillator and program the device into Slave mode for the 002A:

Write a byte “00” of data to Address E0XXXXH with nCS held to ground.

To enable the internal oscillator of 512A/010A, which allows the device to act as either Master or Slave depending on the state of nCS during power-up and reset:

Write a byte “FF” of data to Address 38XXXXH with nCS held to ground.

To enable the internal oscillator of 002A, which allows the device to act as either Master or Slave, depending on the state of nCS during power-up and reset:

Write a byte “FF” of data to Address E0XXXXH with nCS held to ground.

In-System Programming Applications

The AT17LV(A) Series Configurators are in-system (re)programmable. The examples shown on the following pages support the following programmer functions:

1. Reading the Manufacturer’s Code and the Device Code (512-Kbit, and 1-, 2- and 4-Mbit parts only).
2. Programing the device.
3. Verifying the device data.
4. Setting the Reset Polarity option.

While Atmel’s FPGA Configurators can be programmed from various sources (e.g., on-board microcontrollers or PLDs), the applications shown here are designed to facilitate users of our ATDH2200E Configurator Programming Kit and ATDH2225 ISP Direct Download cable. The typical system setup is shown in Figure 2 and Figure 3.

In selecting a device and generating a circuit for any SRAM-based FPGAs, the key issues to address are:

- Number of FPGA program bits versus Configurator data space
- Pinout compatibility and package availability
- Configurator master or slave operation (512A/010A/002A only)
- Existence of weak internal pull-up or pull-down resistors on the inputs of the FPGA or Configurator
- Avoiding contention on the clock line during ISP
- Avoiding contention on the RESET/$\overline{OE}$ ($\overline{OE}$) and $\overline{CE}$ (nCS) lines during ISP (65(A)/128(A)/256(A) only)
- Use of the A2 pin for addressing (up to two Configurators in cascade) or as a chip select (up to *n* Configurators in cascade) during ISP
- Use of the Ready pin, an external Reset signal, and/or an RC constant to delay configuration
- 3-wire (512(A)/010(A)/002(A) only) or 5-wire (65(A)/128(A)/256(A)) ISP interface

Please note that the pages within the configuration EEPROM can be selectively rewritten. It follows that the reset polarity need only be written once. The reset polarity value is latched only during the power-on reset cycle.

The AT17 Series Configurators can interface with many SRAM-based FPGA families. This document is limited to example implementations for the following applications:

1. Atmel AT40K
2. Xilinx® XC3000, XC4000, XC5000, Spartan®, Spartan II, Virtex®, Virtex E and Virtex II
3. Altera® EPF6K, EPF8K, EPF10K, EPF1K and EPF20K

Atmel AT40K and AT6K Applications

All AT6K FPGAs and AT40K FPGAs can be configured with our AT17LV Series Configurators using a simple 3-wire interface that is highly desirable for ISP applications.

Figure 2. Typical System Setup using the ATDH2200 Programmer

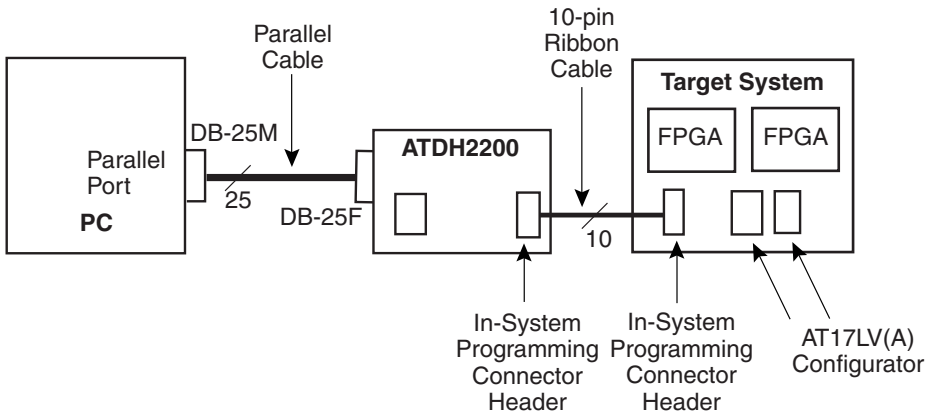
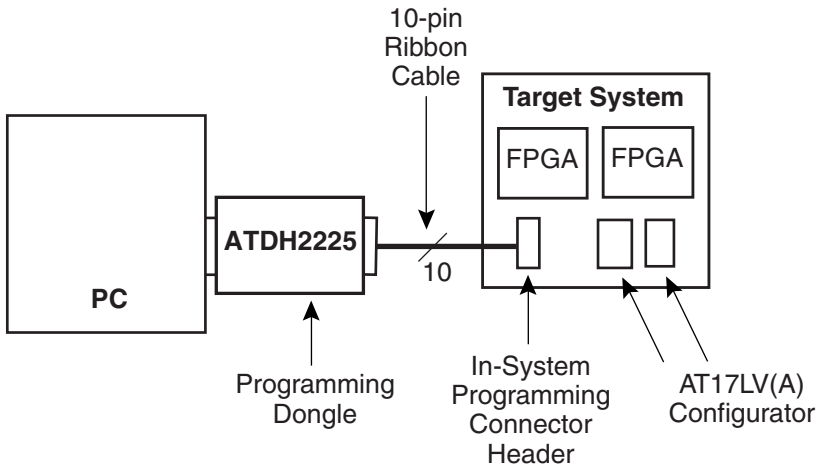


Figure 3. Typical System Setup using the ATDH2225 Download Cable



DC Characteristics in Programming Mode (SER_EN)

V_{CC} = 3.3V - 5V ± 10%, T_A = -40°C - 85°C[1][2]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	4.13	5.25	V
I_{CC}	Supply Current	V_{CC} = 3.6		2.0	5.0	mA
I_{LL}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.4	V
V_{OL}	Output Low-level Voltage	I_{OL} = 2.1 mA			0.4	V

Notes: 1. Commercial temperature range -40°C - 70°C
2. Industrial temperature range -40°C - 85°C

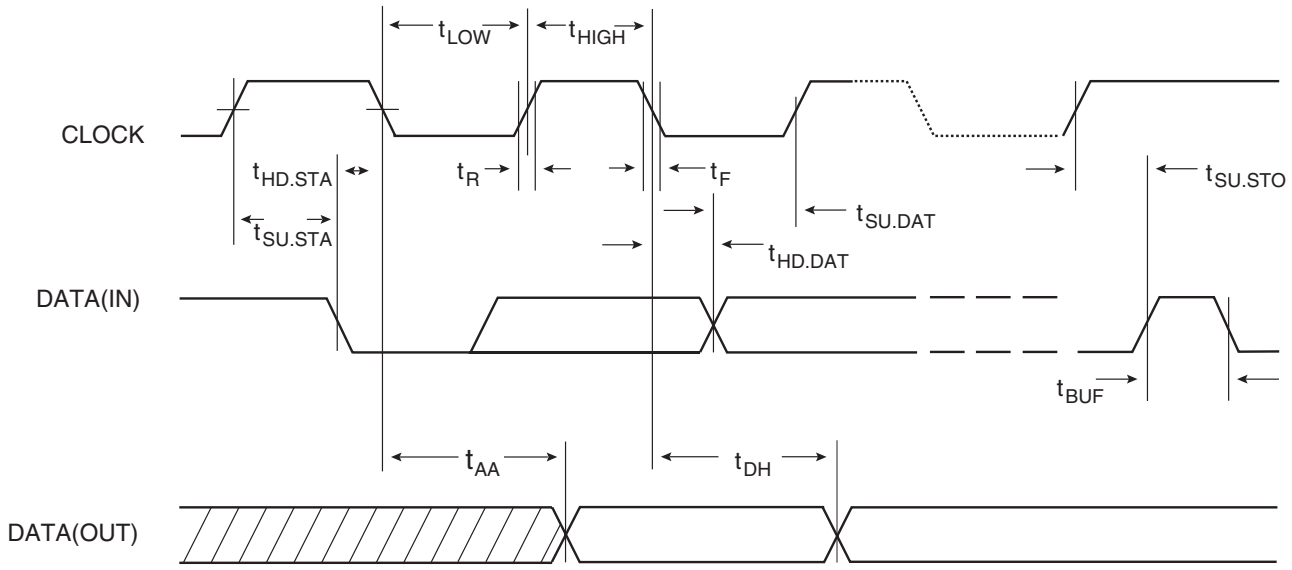
AC Characteristics

V_{CC} = 3.3V - 5V ± 10%, T_A = -40°C - 85°C[1][2]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		400	KHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	1.2		µs
t_{AA}	Clock Low to Data Out Valid		0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD;STA}$	Start Hold Time	0.6		µs
$t_{SU;STA}$	Start Setup Time	0.6		µs
$t_{HD\ DAT}$	Data In Hold Time	0.1		µs
$t_{SU\ DAT}$	Data In Setup Time	0.1		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	0		µs
t_{WR}	Write Cycle Time		25	ms

Notes: 1. Commercial temperature range -40°C - 70°C
2. Industrial temperature range -40°C - 85°C

Figure 4. Serial Data Timing Diagram



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Atmel Configurator Hotline
(408) 436-4119

Atmel Configurator e-mail
configurator@atmel.com

FAQ
Available on web site

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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