AVR32738: AVR32 AP700X Schematic Checklist

Features

- **Power circuit**
- **Reset and wake circuit**
- **USB connection**
- **External bus interface**
- **ABDAC sound DAC interface**
- **JTAG and Nexus debug ports**
- **Clock, crystal oscillator and PLL filter circuits**

1 Introduction

A good hardware design comes from a proper schematic. Since AP7 devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for an AP7 design.

32-bit AVR® Microcontrollers

Application Note

Rev. 32096C-AVR32-09/08

2 Power circuit

2.1 Power supply

Figure 2-1. Power supply example schematic

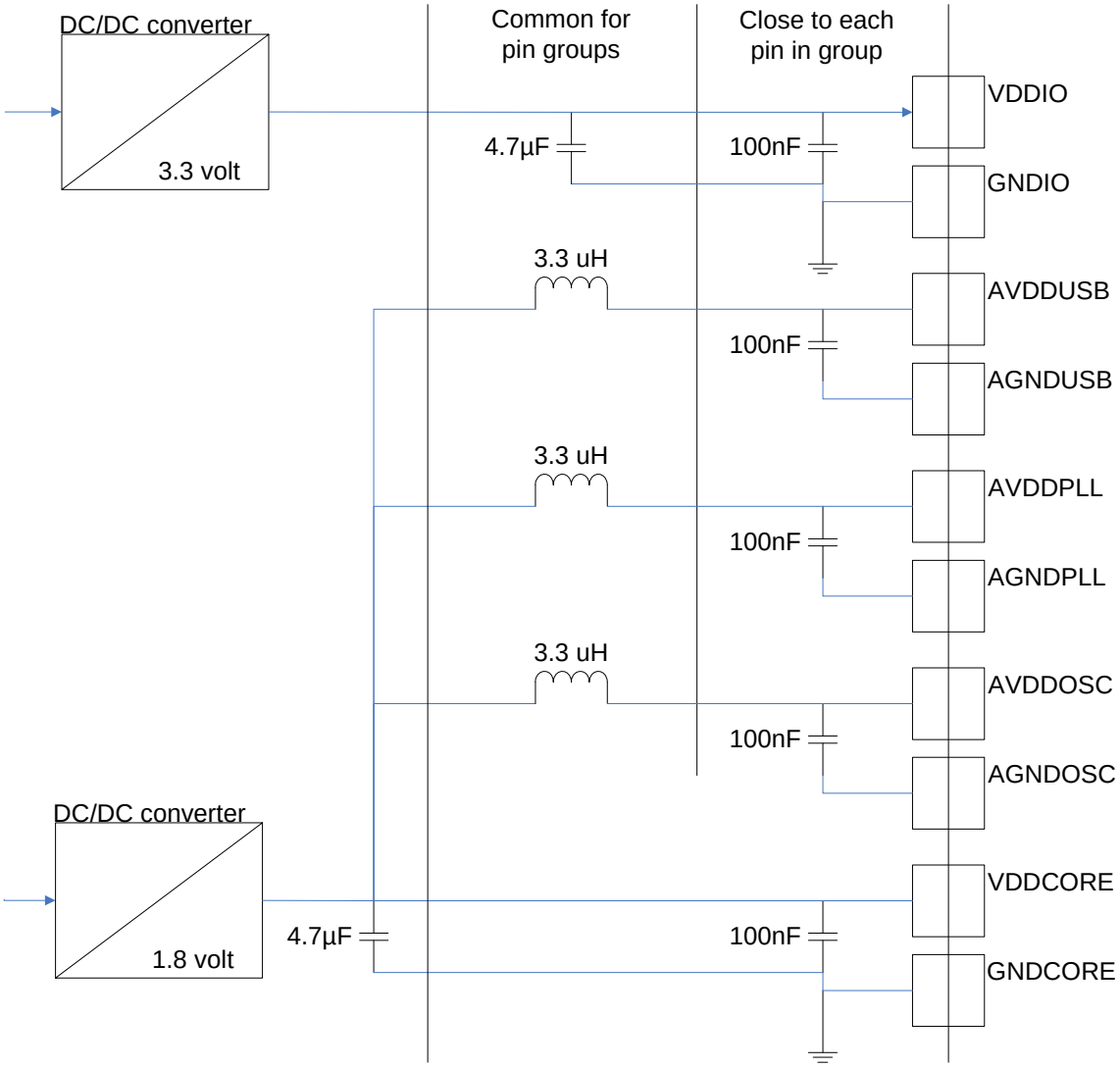

Table 2-1. Power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0 V to 3.6 V Decoupling capacitor 100 nF(1)(2)	Powers I/O lines and USB transceiver. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

☑	Signal name	Recommended pin connection	Description
	AVDDUSB	1.65 V to 1.95 V Decoupling capacitor 100 nF(1)(2) Serial inductor 3.3 µH(1)	Powers the USB. Decoupling/filtering capacitors and serial inductor must be added to improve startup stability and reduce source voltage drop. The inductor may be dropped if USB is not to be used in the design.
	AVDDPLL	1.65 V to 1.95 V Decoupling capacitor 100 nF(1)(2) Serial inductor 3.3 µH(1)	Powers the PLLs. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. The inductor may be dropped if the PLLs are not to be used in the design.
	AVDDOSC	1.65 V to 1.95 V Decoupling capacitor 100 nF(1)(2) Serial inductor 3.3 µH(1)	Powers the oscillators. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDCORE	1.65 V to 1.95 V Decoupling capacitor 100 nF(1)(2)	Powers the core, memories and peripherals. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	AGNDxxx	Connected to ground	Ground pins in a group should be matched with the VDD pins in the same group.
	GNDxxx	Connected to ground	Ground pins in a group should be matched with the VDD pins in the same group.

Note 1: These values are given only as a typical example.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

3 Reset and wake

3.1 Reset circuit

Figure 3-1. Reset circuit example schematic

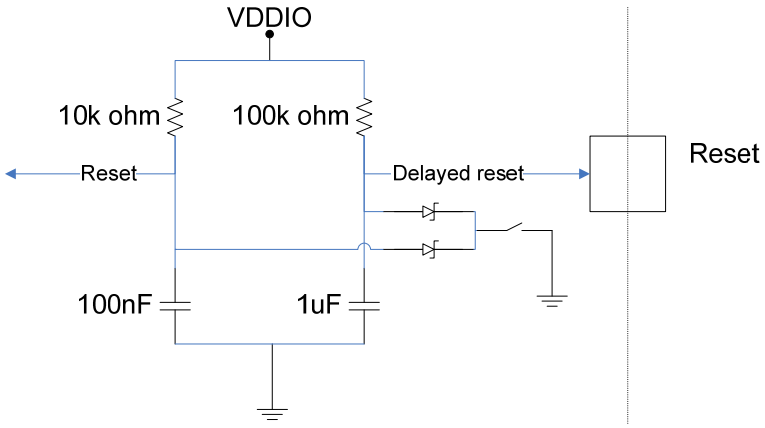

Table 3-1. Reset circuit checklist

☑	Signal name	Recommended pin connection	Description
	RESET	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO. The external reset should in most designs be delayed from the rest of the circuit. This is to assure that external devices are ready when the MCU starts.

3.2 Wake circuit

Figure 3-2. Wake circuit example schematic

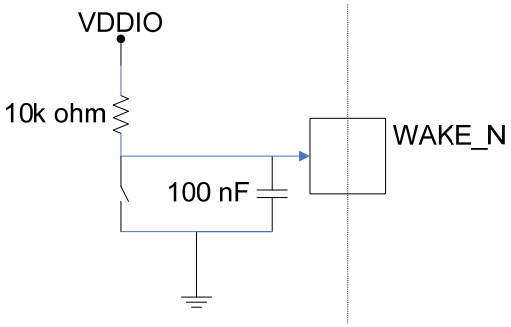

Table 3-2. Wake circuit checklist

☑	Signal name	Recommended pin connection	Description
	WAKE_N	Can be left floating (unconnected) in case no wake from the system needs to be applied to the product	The WAKE_N pin is a Schmitt trigger input integrating a permanent pull-up resistor to VDDIO.

4 Clock, crystal oscillator and PLL filter circuits

4.1 External clock source

Figure 3-3. External clock source schematic

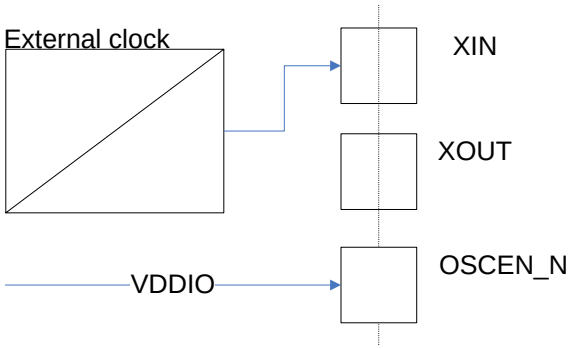

Table 3-3. External clock source checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	1.8 volt (VDDPLL) square wave signal up to 50 MHz on XIN0 and XIN1[(1)], while 32 kHz on XIN32[(2)].
	XOUT	Can be left unconnected	
	OSCEN_N	Connected to VDDIO	OSCEN_N high will disable the internal oscillators.

Note 1: XIN1 **must** be 12 MHz if device is going to use the USB device controller.

Note 2: 32 kHz clock is **mandatory** for device to work.

4.2 Crystal oscillator OSC0, OSC1 and OSC32

Figure 3-4. Crystal oscillator example schematic

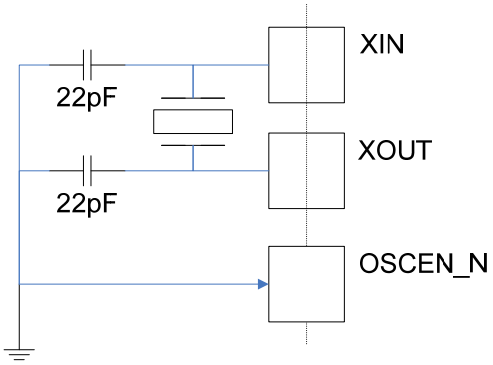

Table 3-4. Crystal oscillator checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22 pF(1)(2)	External crystal between 10 MHz and 27 MHz for XIN0 and XIN1(3), 32 kHz for XIN32(4).
	XOUT	Biasing capacitor 22 pF(1)(2)	
	OSCEN_N	Connected to ground	OSCEN_N low will enable the internal oscillators.

Note 1: These values are given only as a typical example.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

Note 3: XIN1 **must** be 12 MHz if device is going to use the USB device controller.

Note 4: 32 kHz oscillator is **mandatory** for device to work.

4.3 PLL filter

Figure 3-5. PLL filter example schematic

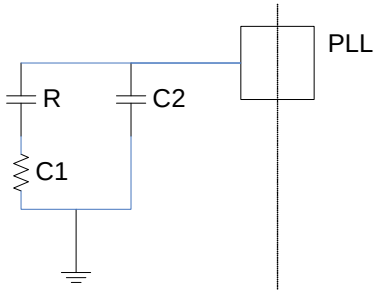

Table 3-5. PLL filter checklist

☑	Signal name	Recommended pin connection	Description
	PLL	Passive RC filter resistor R(1) and capacitors C1(1) and C2(1).	See the Excel spreadsheet ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip (available on the Atmel Web site) to calculate the best R, C1 and C2 component values for the PLL loop back filter.

Note 1: Components should be placed as close as possible to the PLL pin, vias should be avoided.

5 USB connection

5.1 Device mode, powered from bus connection

Figure 5-1. USB in device mode, bus powered connection example schematic

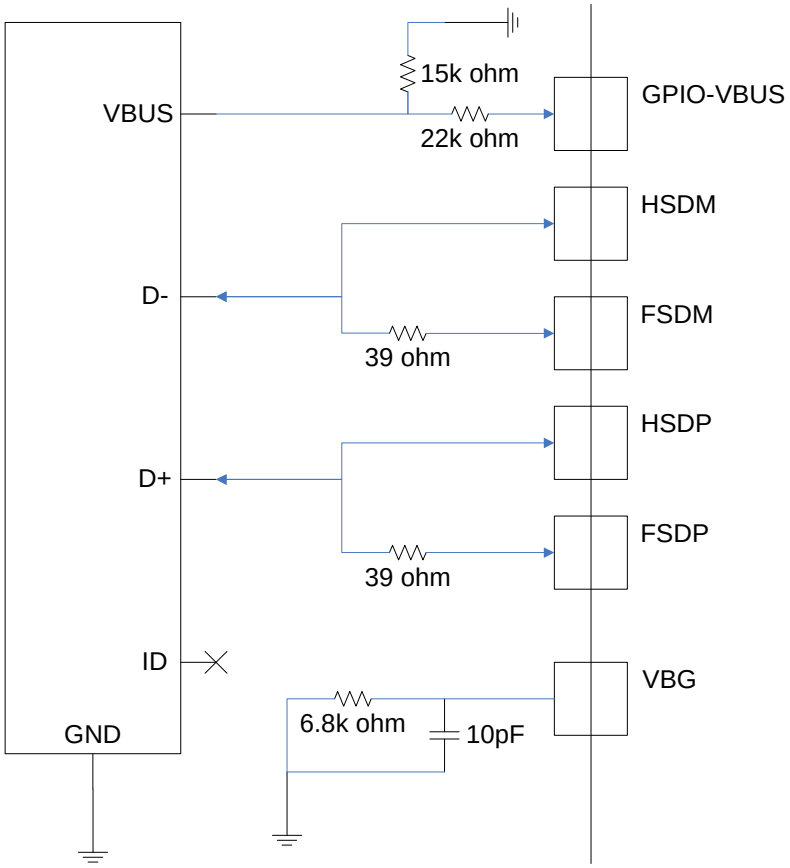

Table 5-1. USB bus powered connection checklist

☑	Signal name	Recommended pin connection	Description
	GPIO-VBUS	Can be left unconnected Use a 22k ohm + 15k ohm voltage divider to limit the voltage to 3.3 V.	USB power measurement pin. The GPIO pin can be used to trigger a USB plug connection or disconnection.
	HSDM	Directly to connector	High speed USB interface data -
	FSDM	39 ohm series resistor Placed as close as possible to pin	Full speed USB interface data -
	HSDP	Directly to connector	High speed USB interface data +
	FSDP	39 ohm series resistor Placed as close as possible to pin	Full speed USB interface data +
	VBG	Connected to a 6810 ohm 0.5%(1) resistor and a 10 pF(1) capacitor	USB bandgap.

Note 1: Component should be placed as close as possible to pin, vias should be avoided.

6 Ethernet interface

When designing in the Ethernet physical device (PHY) the designer should refer to the datasheet for the PHY. This datasheet usually contains layout advice, connection schematics, reference design, etc.

The information in the PHY datasheet is vital to get optimal performance and stability.

6.1 Ethernet interface in MII mode

Figure 6-1. Ethernet interface in MII mode example schematic

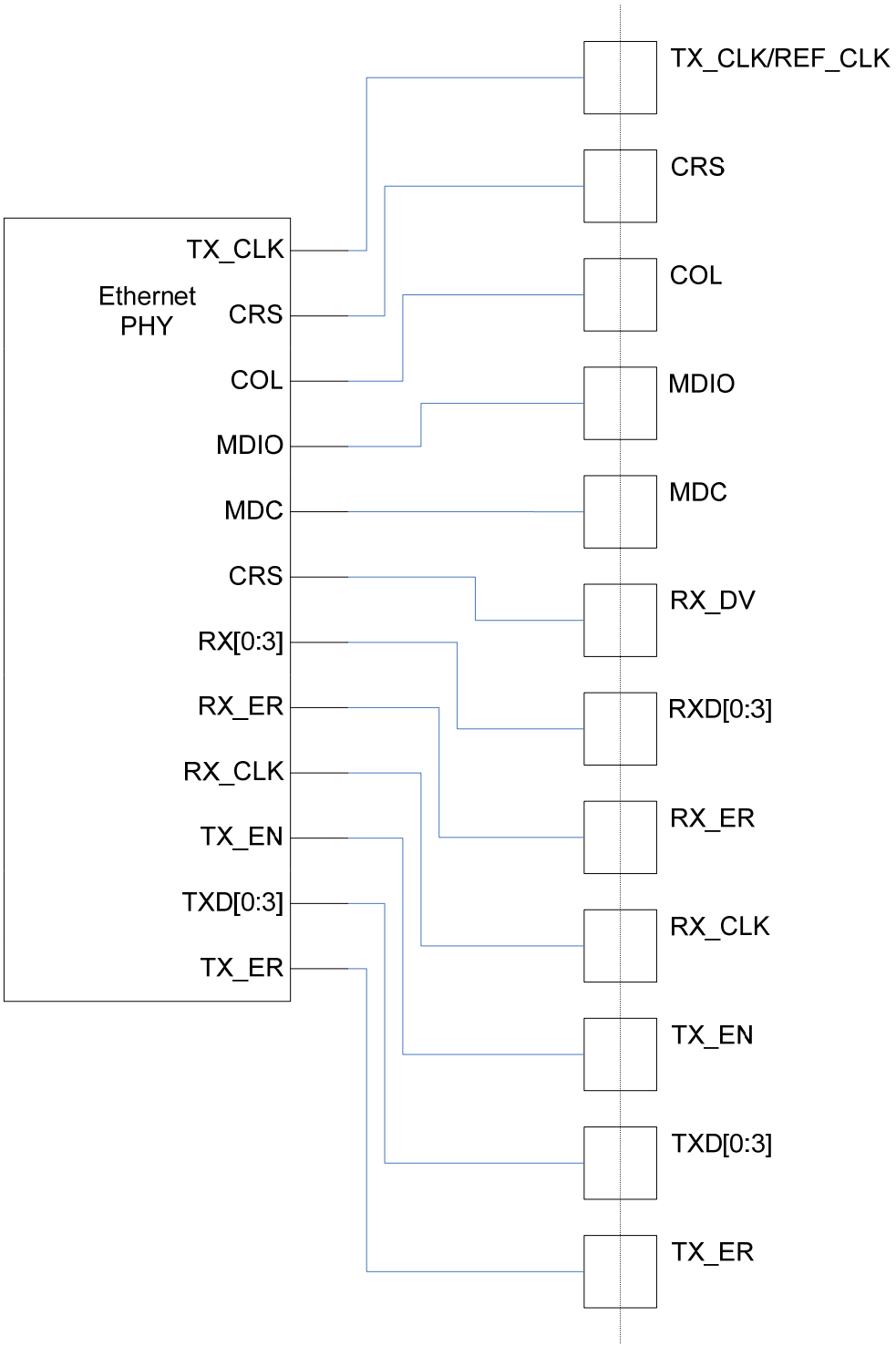

Table 6-1. Ethernet interface in MII mode checklist

☑	Signal name	Recommended pin connection	Description
	TX_CLK/ REF_CLK		Transmit clock, 25 MHz for 100 Mb/s data rate
	CRS		Carrier sense
	COL		Collision detect
	MDIO		PHY maintenance data
	MDC		PHY maintenance clock
	RX_DV		Receive data valid
	RXD[0:3]		Receive data 4-bit
	RX_ER		Receive error
	RX_CLK		Receive clock, 25 MHz for 100 Mb/s data rate
	TX_EN		Transmit enable
	TXD[0:3]		Transmit data 4-bit
	TX_ER		Transmit error

6.2 Ethernet interface in RMII mode

Figure 6-2. Ethernet interface in RMII mode example schematic

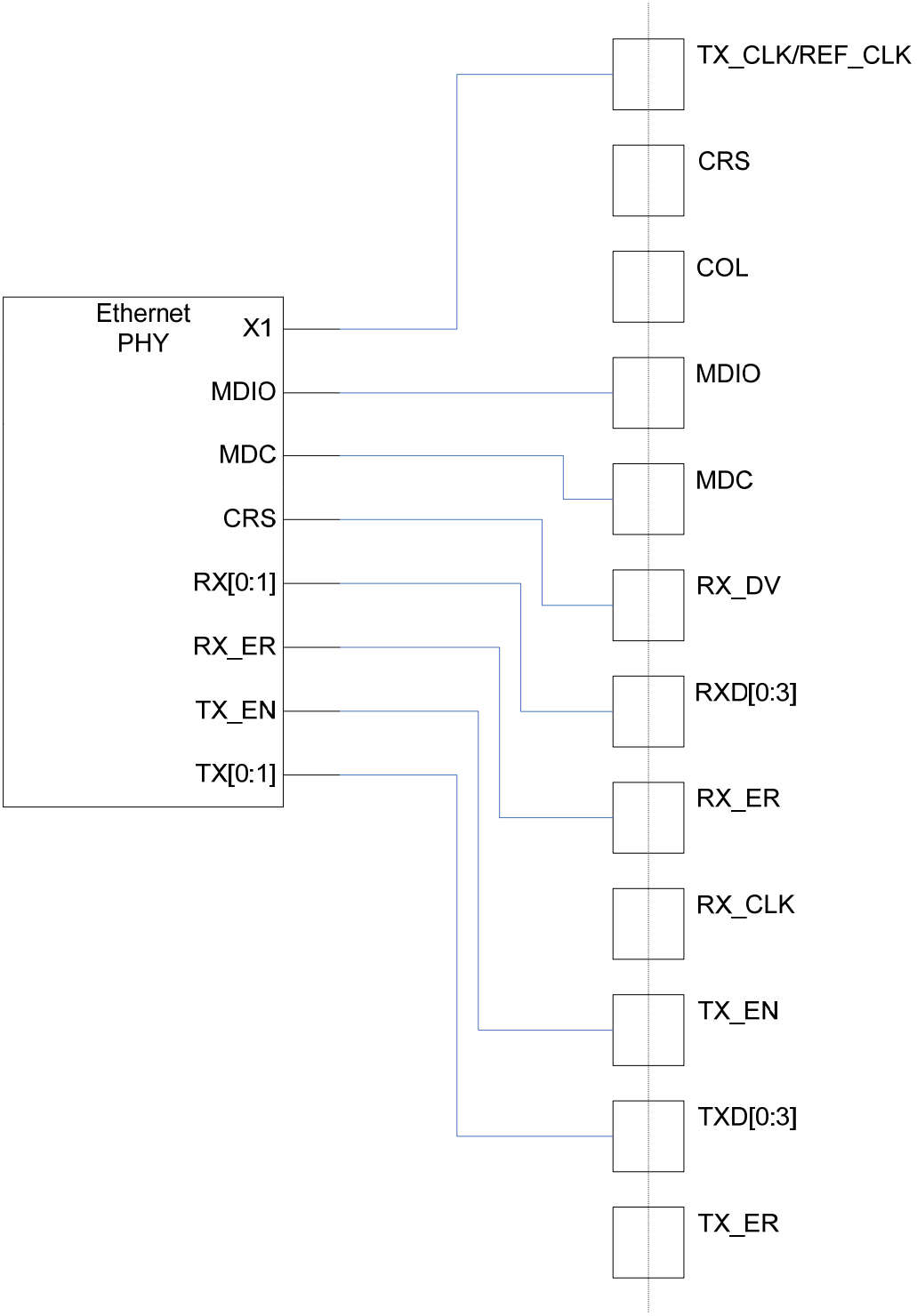

Table 6-2. Ethernet interface in RMII mode checklist

☑	Signal name	Recommended pin connection	Description
	TX_CLK/ REF_CLK		Reference clock, 50 MHz for 100 Mb/s data rate
	CRS	Not used in RMII mode	
	COL	Not used in RMII mode	
	MDIO		PHY maintenance data
	MDC		PHY maintenance clock
	RX_DV		Carrier sense, data valid
	RXD[0:1]		Receive data 2-bit
	RXD[2:3]	Not used in RMII mode	
	RX_ER		Receive error
	RX_CLK	Not used in RMII mode	
	TX_EN		Transmit enable
	TXD[0:1]		Transmit data 2-bit
	TXD[2:3]	Not used in RMII mode	
	TX_ER	Not used in RMII mode	

7 External bus interface

7.1 Static memory

7.1.1 32-bit static memory

Table 7-1. 32-bit static memory pin wiring

☑	SMC EBI signal	32-bit static memory
	D[0:31]	D[0:31]
	A[2:25](1)	A[0:23]
	NBS0 (A[0])	Byte enable 0
	NBS1 (NWR[1])	Byte enable 1
	NBS2 (A[1])	Byte enable 2
	NBS3 (NWR[3])	Byte enable 3
	NWR0	WE
	NRD	OE
	NWAIT	WAIT
	NCSx	CS

Notes: 1. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.1.2 16-bit static memory

Table 7-2. 16-bit static memory pin wiring

☑	SMC EBI signal	16-bit static memory

☑	SMC EBI signal	16-bit static memory
	D[0:15]	D[0:15]
	A[1:25](1)	A[0:24]
	NBS0 (A[0])	Byte enable low
	NBS1 (NWR[1])	Byte enable high
	NWR0	WE
	NRD	OE
	NWAIT	WAIT
	NCSx	CS

Notes: 2. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.1.3 2 x 16-bit static memory

Table 7-3. 2 x 16-bit static memory pin wiring

☑	SMC EBI signal	16-bit static memory	16-bit static memory
	D[0:15]	D[0:15]	
	D[16:31]		D[0:15]
	A[2:25](1)	A[0:23]	A[0:23]
	NBS0 (A[0])	Byte enable low	
	NBS1 (NWR[1])	Byte enable high	
	NBS2 (A[1])		Byte enable low
	NBS3 (NWR[3])		Byte enable high
	NWR0	WE	WE
	NRD	OE	OE
	NWAIT	WAIT	WAIT
	NCSx	CS	CS

Notes: 1. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.1.4 8-bit static memory

Table 7-4. 8-bit static memory pin wiring

☑	SMC EBI signal	8-bit static memory
	D[0:7]	D[0:7]
	A[0:25](1)	A[0:25]
	NWR0	WE
	NRD	OE
	NWAIT	WAIT
	NCSx	CS

Notes: 1. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.1.5 2 x 8-bit static memory

Table 7-5. 2 x 8-bit static memory pin wiring

☑	SMC EBI signal	8-bit static memory	8-bit static memory
	D[0:7]	D[0:7]	
	D[8:15]		D[0:7]
	A[1:25](1)	A[0:24]	A[0:24]
	NWR0	WE	
	NWR1		WE
	NRD	OE	OE
	NWAIT	WAIT	WAIT
	NCSx	CS	CS

Notes: 1. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.1.6 4 x 8-bit static memory

Table 7-6. 4 x 8-bit static memory (SM) pin wiring

☑	SMC EBI signal	8-bit SM	8-bit SM	8-bit SM	8-bit SM
	D[0:7]	DQ[0:7]			
	D[8:15]		DQ[0:7]		
	D[16:23]			DQ[0:7]	
	D[24:31]				DQ[0:7]
	A[2:25](1)	A[0:23]	A[0:23]	A[0:23]	A[0:23]
	NWR0	WE			
	NWR1		WE		
	NWR2 (A[1])			WE	
	NWR3				WE
	NRD	OE	OE	OE	OE
	NWAIT	WAIT	WAIT	WAIT	WAIT
	NCSx	CS	CS	CS	CS

Notes: 1. When using address A[23:25] on PORTE the I/O lines must have a 5k ohm pull-down to ground for the static memory device to work as intended during boot.

7.2 SDRAM

7.2.1 32-bit SDRAM

Table 7-7. 32-bit SDRAM pin wiring

☑	SMC EBI signal	32-bit SDRAM
	D[0:31]	DQ[0:31]
	A[2:11]	A[0:9]
	SDA10	A[10]
	A[13:14]	A[11:12]

☑	SMC EBI signal	32-bit SDRAM
	BA[0:1]	BA[0:1]
	SDCK	CLK
	SDCKE	CKE
	SDWE	WE
	RAS	RAS
	CAS	CAS
	NBS0 (A[0])	DQM0
	NBS1 (NWR[1])	DQM1
	NBS2 (A[1])	DQM2
	NBS3 (NWR[3])	DQM3
	SDCS (NCS1)	CS

7.2.2 16-bit SDRAM

Table 7-8. 16-bit SDRAM pin wiring

☑	SMC EBI signal	16-bit SDRAM
	D[0:15]	DQ[0:15]
	A[2:11]	A[0:9]
	SDA10	A[10]
	A[13:14]	A[11:12]
	BA[0:1]	BA[0:1]
	SDCK	CLK
	SDCKE	CKE
	SDWE	WE
	RAS	RAS
	CAS	CAS
	NBS0 (A[0])	DQML
	NBS1 (NWR[1])	DQMH
	SDCS (NCS1)	CS

7.2.3 2 x 16-bit SDRAM

Table 7-9. 2 x 16-bit SDRAM pin wiring

☑	SMC EBI signal	16-bit SDRAM	16-bit SDRAM
	D[0:15]	DQ[0:15]	
	D[16:31]		DQ[0:15]
	A[2:11]	A[0:9]	A[0:9]
	SDA10	A[10]	A[10]
	A[13:14]	A[11:12]	A[11:12]
	BA[0:1]	BA[0:1]	BA[0:1]
	SDCK	CLK	CLK

☑	SMC EBI signal	16-bit SDRAM	16-bit SDRAM
	SDCKE	CKE	CKE
	SDWE	WE	WE
	RAS	RAS	RAS
	CAS	CAS	CAS
	NBS0 (A[0])	DQML	
	NBS1 (NWR[1])	DQMH	
	NBS2 (A[1])		DQML
	NBS3 (NWR[3])		DQMH
	SDCS (NCS1)	CS	CS

7.2.4 2 x 8-bit SDRAM

Table 7-10. 2 x 8-bit SDRAM pin wiring

☑	SMC EBI signal	8-bit SDRAM	8-bit SDRAM
	D[0:7]	DQ[0:7]	
	D[7:15]		DQ[0:7]
	A[2:11]	A[0:9]	A[0:9]
	SDA10	A[10]	A[10]
	A[13:14]	A[11:12]	A[11:12]
	BA[0:1]	BA[0:1]	BA[0:1]
	SDCK	CLK	CLK
	SDCKE	CKE	CKE
	SDWE	WE	WE
	RAS	RAS	RAS
	CAS	CAS	CAS
	NBS0 (A[0])	DQM	
	NBS1 (NWR[1])		DQM
	SDCS	CS	CS

7.2.5 4 x 8-bit SDRAM

Table 7-11. 4 x 8-bit SDRAM pin wiring

☑	SMC EBI signal	8-bit SDRAM	8-bit SDRAM	8-bit SDRAM	8-bit SDRAM
	D[0:7]	DQ[0:7]			
	D[7:15]		DQ[0:7]		
	D[16:23]			DQ[0:7]	
	D[24:31]				DQ[0:7]
	A[2:11]	A[0:9]	A[0:9]	A[0:9]	A[0:9]
	SDA10	A[10]	A[10]	A[10]	A[10]
	A[13:14]	A[11:12]	A[11:12]	A[11:12]	A[11:12]
	BA[0:1]	BA[0:1]	BA[0:1]	BA[0:1]	BA[0:1]

☑	SMC EBI signal	8-bit SDRAM	8-bit SDRAM	8-bit SDRAM	8-bit SDRAM
	SDCK	CLK	CLK	CLK	CLK
	SDCKE	CKE	CKE	CKE	CKE
	SDWE	WE	WE	WE	WE
	RAS	RAS	RAS	RAS	RAS
	CAS	CAS	CAS	CAS	CAS
	NBS0 (A[0])	DQM			
	NBS1 (NWR[1])		DQM		
	NBS2 (A[1])			DQM	
	NBS3 (NWR[3])				DQM
	SDCS	CS	CS	CS	CS

7.3 CompactFlash

Table 7-12. 8-bit and 16-bit CompactFlash pin wiring

☑	SMC EBI signal	16-bit CompactFlash
	D[0:7]	D[0:7]
	D[8:15](1)	D[8:15]
	A[0:10]	A[0:10]
	A[22]	REG
	NSC[4](2)	CFCS[0]
	NSC[5](2)	CFCS[1]
	NRD	OE
	NWR0	WE
	NWR1	IOR
	NWR3	IOW
	CFRNW(2)	CFRNW
	CFCE1	CE1
	CFCE2	CE2
	NWAIT	WAIT
	PIO[n](3)	CD1 or CD2

Notes:
1. Only needed for 16-bit CompactFlash.
2. Not directly connected to the CompactFlash slot. Permits control of a bidirectional buffer between the EBI and the CompactFlash slot.
3. Any PIO line.

7.4 NAND

Table 7-13. 8-bit and 16-bit NAND pin wiring

☑	SMC EBI signal	8-bit NAND
	D[0:7]	I/O[0:7]
	D[8:15](1)	I/O[8:15]

☑	SMC EBI signal	8-bit NAND
	A[21]	CLE
	A[22]	ALE
	NANDOE	RE
	NANDWE	WE
	NCS[3]	CE
	GPIO[n](2)	R/B

Notes: 1. Only needed for 16-bit NAND.
2. Any PIO line.

8 ABDAC stereo sound DAC interface

8.1 Directly connected speakers

Figure 8-1. Directly connected speakers example schematic

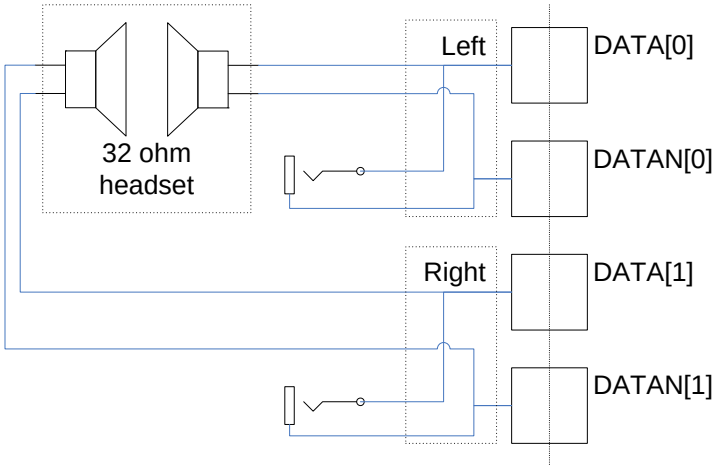

Table 8-1. Directly connected speakers checklist

☑	Signal name	Recommended pin connection	Description
	DATA[0]	Can be directly connected for testing purposes	Current limited by device pad. Speaker must be connected between DATA[0] and DATAN[0] for best signal to noise ratio.
	DATAN[0]	Can be directly connected for testing purposes	Current limited by device pad. Speaker must be connected between DATA[0] and DATAN[0] for best signal to noise ratio.
	DATA[1]	Can be directly connected for testing purposes	Current limited by device pad. Speaker must be connected between DATA[1] and DATAN[1] for best signal to noise ratio.
	DATAN[1]	Can be directly connected for testing purposes	Current limited by device pad. Speaker must be connected between DATA[1] and DATAN[1] for best signal to noise ratio.

8.2 Line out with passive filter

Figure 8-2. Line out with passive filter example schematic

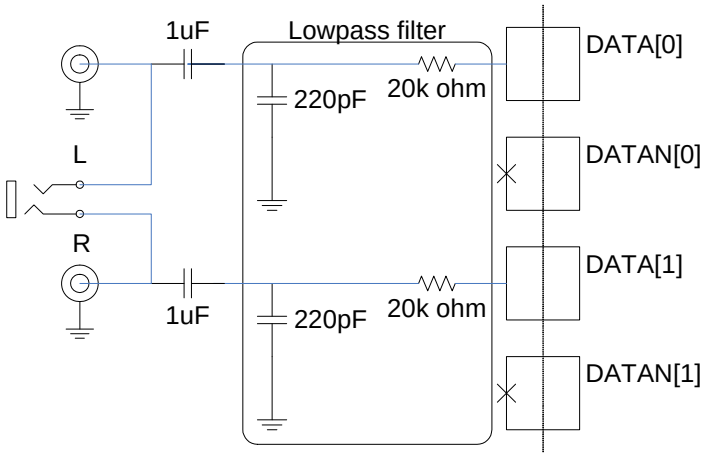

Table 8-2. Line out with passive filter checklist

☑	Signal name	Recommended pin connection	Description
	DATA[0]	Connected to low pass filter and 1 µF capacitor to remove DC bias	
	DATAN[0]	Not in use	
	DATA[1]	Connected to low pass filter and 1 µF capacitor to remove DC bias	
	DATAN[1]	Not in use	

8.3 High power output with external amplifier

Figure 8-3. High power output with external amplifier example schematic

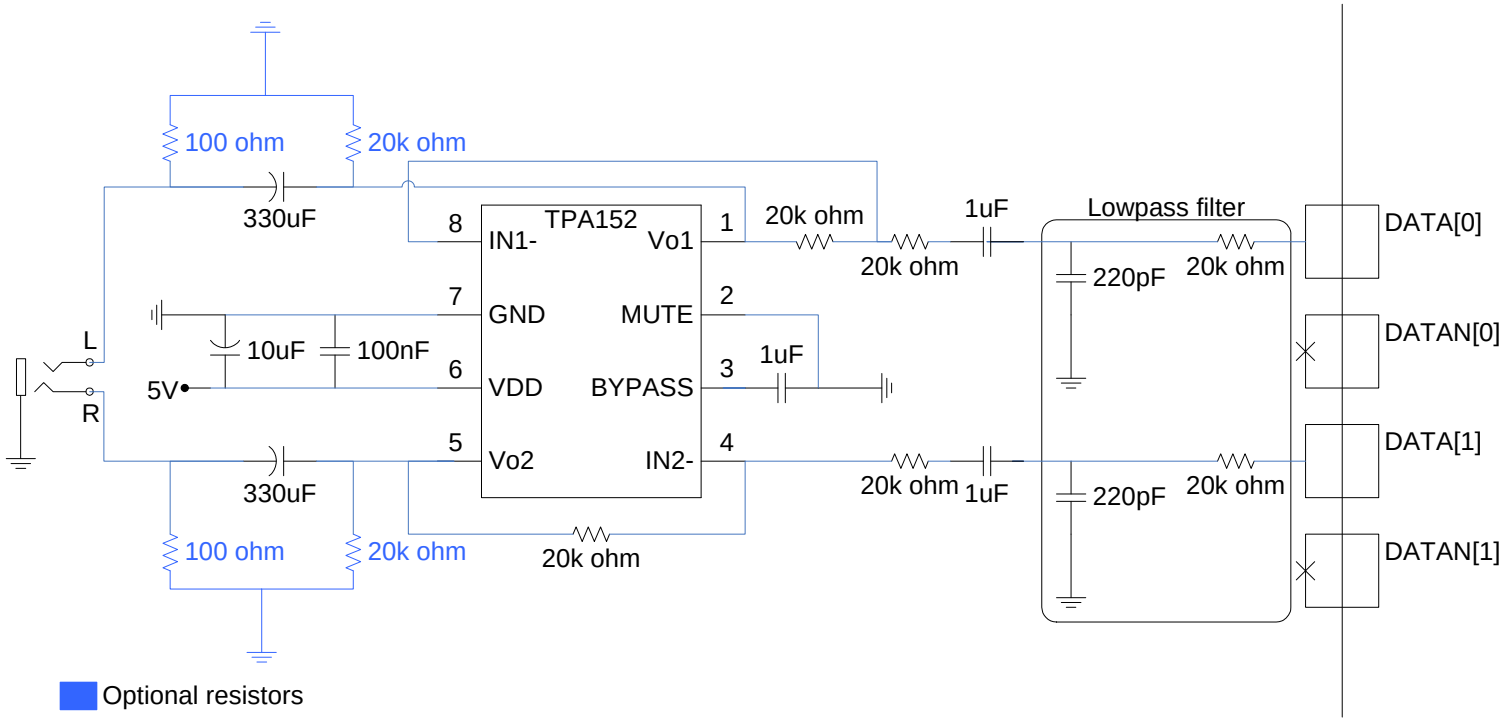

Table 8-3. High power output with external amplifier checklist

☑	Signal name	Recommended pin connection	Description
	DATA[0]	Connected to low pass filter and external amplifier	
	DATAN[0]	Not in use	
	DATA[1]	Connected to low pass filter and external amplifier	
	DATAN[1]	Not in use	

9 JTAG and Nexus debug ports

9.1 JTAG port interface

Figure 9-1. JTAG port interface example schematic

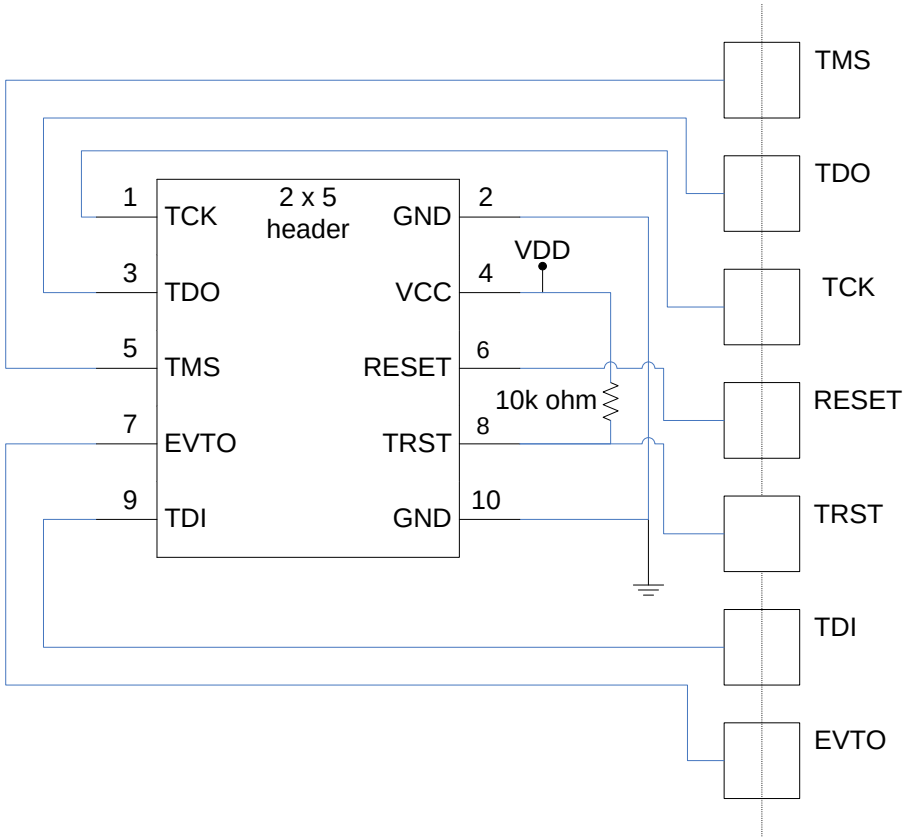

Table 9-1. JTAG port interface checklist

☑	Signal name	Recommended pin connection	Description
	TMS		Test mode select, sampled on rising TCK.
	TDO		Test data output, driven on falling TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	RESET		Device external reset line.
	TDI		Test data input, sampled on rising TCK.
	EVTO		Event output.
	TRST		Test reset.

9.2 Nexus port interface

Figure 9-2. Nexus port interface example schematic

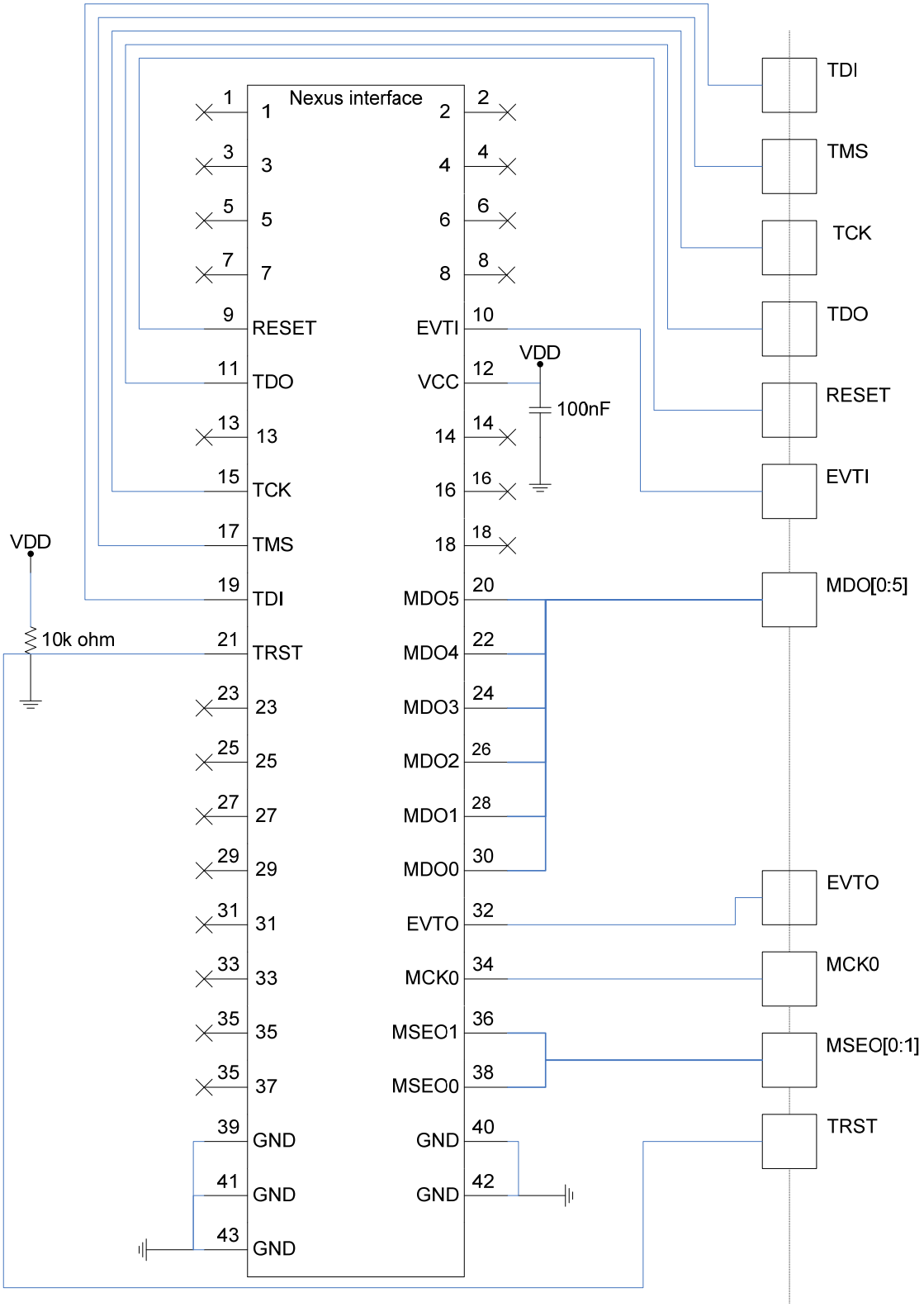

Table 9-2. Nexus port interface checklist

☑	Signal name	Recommended pin connection	Description
	TDI		Test data input, sampled on rising TCK.
	TMS		Test mode select, sampled on rising TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	TDO		Test data output, driven on falling TCK.
	RESET		Device external reset line.
	EVTI		Event input.
	MDO[0:5]		Trace data output.
	EVTO		Event output.
	MCK0		Trace data output clock.
	MSE[0:1]		Trace frame control.

10 Suggested reading

10.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR32 in the *Datasheets* section.

10.2 Evaluation kit schematic

The starter kit STK®1000/STK1002 and reference design NGW100 contains a full schematic for the boards; they can be used as a reference design. The schematics are available on http://www.atmel.com/AVR32 in the *Tools & Software* section.

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