a

CMOS 180 MHz Quadrature Digital Upconverter

Preliminary Technical Information

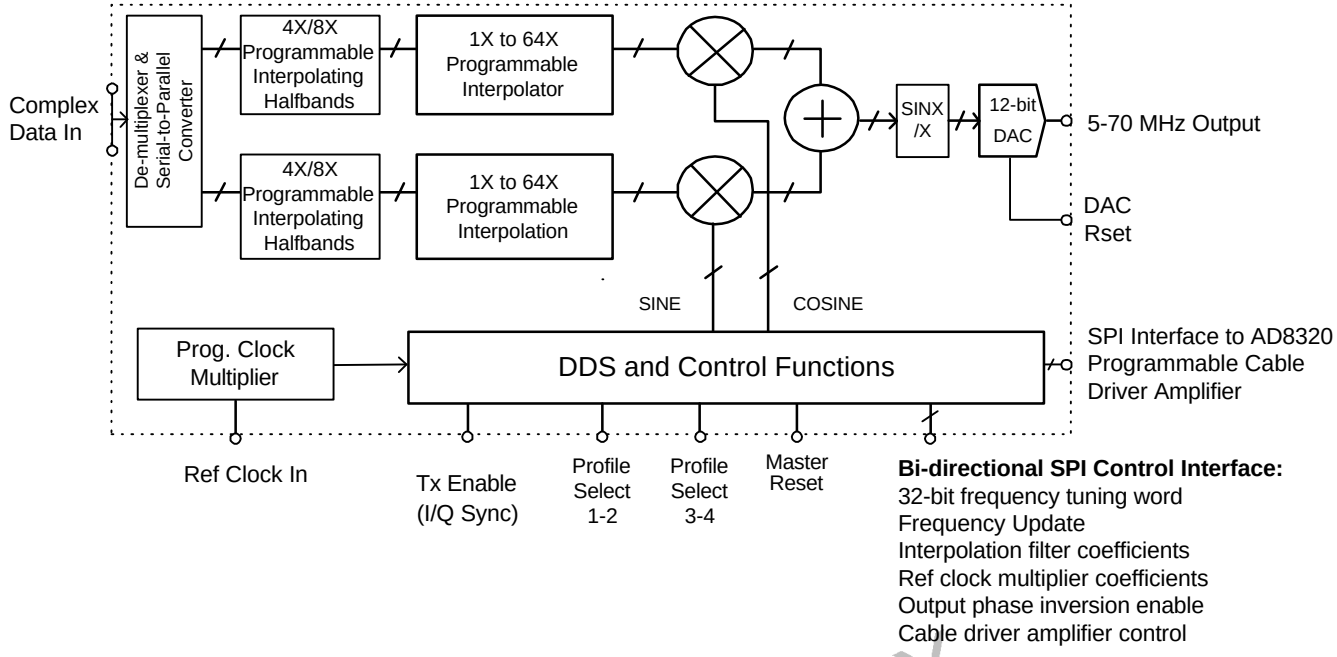
AD9856

FEATURES

Universal low-cost solution for HFC network return-channel Tx function
Up to 70 MHz output bandwidth
Integrated 12-bit D/A converter
Programmable sample rate interpolation filter
Programmable reference clock multiplier
Internal SINX/X Compensation filter
>52 dB SFDR @40 MHz Analog DAC Out
>48 dB SFDR @70 MHz Analog DAC Out
>80 dB narrowband SFDR @ 70 MHz Aout
+3.3V Single Supply Operation
Low power: 400 mW@ max. clock speed
Space-saving surface-mount packaging
Bi-directional control bus interface
Supports burst and continuous Tx modes
4 stored pin-selectable modulator profiles
Direct interface to AD8320 PGA cable driver

APPLICATIONS

HFC Data, Telephony, and Video Modems
Wireless and satellite communications



FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9856 integrates a high-speed direct-digital synthesizer (DDS), a high-performance, high-speed 12-bit Digital-to-Analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions onto a single chip, to form a complete quadrature digital upconverter device. The AD9856 is primarily intended to function as a universal upstream and downstream I/Q modulator for interactive HFC cable network applications, where cost, size, power dissipation, and dynamic performance are critical attributes.

The AD9856 is fabricated on an advanced CMOS process and it delivers an exceptional level of mixed signal performance. The device provides a precision digital modulation and upconvert function with a direct interface port to the AD8320, digitally-programmable cable driver amplifier. The AD9853/AD8320 chipset forms a highly-integrated, low-power, small footprint, and cost-effective solution for the HFC return-path Tx requirement.

The AD9856 is available in a space-saving surface mount package and is specified to operate over the extended industrial temperature range of -40° to +85°C.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS[1]

Maximum Junction Temp. .....+165°C
Vs ..... +6V
Digital Inputs ..... -0.7V to +Vs
Digital Output Current 5mA
Storage Temperature ..... -65°C to +150°C
Operating Temp. ..... -40°C to +85°C
Lead Temp. (10 sec. soldering) ..... +300°C

AD9856 ELECTRICAL CHARACTERISTICS (Vs=+3.3 V ±5%, Rset=3.9 k Ω, Reference Clock Frequency = 8.0 MHz with internal PLL enabled @ 20X).

Parameter	Temp	Test Level	AD9856 Min	AD9856 Typ	AD9856 Max	Units
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
PLL Disabled	FULL	VI			180.0	MHz
PLL Enabled @ 20X	FULL	VI			9.0	MHz
PLL Enabled @ 4X	FULL	VI			45	MHz
Duty Cycle	+25°C	I		50		%
Input Capacitance	+25°C	IV		3		pF
Input Impedance	+25°C	IV		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				12		Bits
Full Scale Output Current	+25°C	V	5	10	20	mA
Gain Error	+25°C	I	-10		+10	%FS
Output Offset	+25°C	I			10	uA
Differential Non-linearity	+25°C	I		.5		lsb
Integral Non-linearity	+25°C	I		1		lsb
Output Capacitance	+25°C	I		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz Aout[3]	+25°C	I		-100		dBc
Voltage Compliance Range	+25°C	I	0		1.5	V
Wideband SFDR:						
1 MHz Analog Out	+25°C	V		65		dBc
20 MHz Analog Out	+25°C	V		60		dBc
40 MHz Analog Out	+25°C	V		55		dBc
65 MHz Analog Out	+25°C	V		52		dBc
70 MHz Analog Out	+25°C	V		50		dBc
MODULATOR CHARACTERISTICS						
I/Q Offset	+25°C	I		48		dB
Error Vector Magnitude	+25°C	I		1		%
Pass Band Amplitude Ripple	+25°C	I		±0.3		dB
TIMING CHARACTERISTICS						
Output Latency of Profile Change			15			Fmax Cycles
Wake-up Time from Full Sleep Mode				10		uS

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AD9856 ELECTRICAL CHARACTERISTICS (Vs=+3.3V±5%, Rset=3.9 k Ω, Reference Clock Frequency = 8.0 MHz with internal PLL enabled @ 20X).

Parameter	Temp	Test Level	AD9856 Min	AD9856 Typ	AD9856 Max	Units
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	I	+2.7			V
Logic "0" Voltage	+25°C	I			+0.4	V
Logic "1" Current	+25°C	IV			12	uA
Logic "0" Current	+25°C	IV			12	uA
Input Capacitance	+25°C	V		3		pF
POWER SUPPLY						
+Vs Current @ Full Operating Conditions	+25°C	I		121		mA
P_{DISS} @ Full Operating Conditions	+25°C	I		400		mW
P_{DISS} @ Non-Bursting	+25°C	I		40		mW
P_{DISS} @ Full Power-down Mode	+25°C	I		1		mW

PRELIMINARY TECHNICAL DATA

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]DC to 70 MHz output bandwidth.
[3]Residual phase noise
[4]Excluding aliased frequency components

EXPLANATION OF TEST LEVELS

Test Level
I - 100% Production Tested.
III - Sample Tested Only.
IV - Parameter is guaranteed by design and characterization testing.
V - Parameter is a typical value only.
VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

Table I. MODULATOR FUNCTION DESCRIPTION

Input Data Format	12-bit parallel, 6-bit nibble, 3-bit nibble - selectable via control bus. Input data is assumed to be 4X oversampled when input to the AD9856.
Input Sample Rate	Min: CLK/512; max: 45 MS/s. Programmable via control bus.
Input Reference Clock Frequency	For 5-70 MHz Aout operation (160 MHz internal reference clock): w/PLL enabled: 8 - 20 MHz, programmable via control bus w/PLL disabled: 160 MHz Note: For optimum data synchronization, the AD9856 Reference Clock, and the input data clock, should be derived from the same clock source.
Internal Reference Clock PLL	Programmable in integer steps over the range of 4X-20X; enable/disable control via control bus
Profile Select	Four pin-selectable, pre-programmed, modulator formats
Interpolating range	Fixed 4X, programmable 2X, and programmable 64X
Halfband Filters	Interpolating filters that compensate for CIC passband rolloff characteristics
Tx Enable Function - Burst Mode	When Burst Mode is enabled via the control bus, the rising edge of the applied Tx Enable pulse should be coincident with, and frame, the input data packet. This establishes data sampling synchronization.
Tx Enable Function - Continuous Mode	When continuous mode is enabled via the control bus, the Tx Enable pin becomes the I/Q demux control. Logic “1” outputs the demux to the I channel; logic “0” outputs the demux to the Q channel.
SINX/X filter	Pre-compensates for SINX/X roll-off of DAC; user bypassable.
I/Q Channel Invert	COS - j SIN or COS + j SIN, selectable via control bus

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Table II. PACKAGE LEAD FUNCTION ASSIGNMENTS (PRELIMINARY)

Pin #	Pin Name	Pin Function
1	Tx Enable	Input pulse that frames the burst data stream
2	D11	Input data
3	D10	Input data
4	DVDD	Digital supply voltage
5	DGND	Digital ground
6	D9	Input data
7	D8	Input data
8	D7	Input data
9	D6	Input data
10	DVDD	Digital supply voltage
11	DGND	Digital ground
12	D5	Input data
13	D4	Input data
14	D3	Input data
15	D2	Input data
16	D1	Input data
17	D0	Input data
18	N/C	No internal connection
19	N/C	No internal connection
20	DGND	Digital ground
21	DVDD	Digital supply voltage
22	N/C	No internal connection
23	AGND	Analog ground
24	REF Bypass	Bypass with .01 µF CAP

Pin #	Pin Name	Pin Function
25	DAC Rset	R_{SET} resistor connection
26	DAC Baseline	DAC baseline voltage
27	AVDD	Analog supply voltage
28	AGND	Analog ground
29	IOUTB	Complementary analog current output of the DAC
30	IOUT	True analog current output of DAC
31	AGND	Analog ground
32	PLL GND	PLL ground
33	PLL Filter	PLL loop filter connection
34	PLL Supply	PLL voltage supply
35	CA Enable	Cable driver amp enable
36	CA Data	Cable driver amp data
37	CA CLK	Cable driver amp clock
38	CS(B)	Chip select (bar)
39	SDO	Serial data output
40	SD I/O	Serial port I/O
41	SCLK	Serial port clock
42	I/O Reset	Performs I/O synchronization
43	DGND	Digital ground
44	DVDD	Digital supply voltage
45	PS0	Profile select 1
46	PS1	Profile select 2
47	REF CLK	Reference clock input
48	RESET	Master Reset

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Table III. Control Bus Register Definitions.

Bit name	Width	Position	Description	Profile	Address (Hex)
SDO Active	1	<7>	Active high indicates serial port uses dedicated in/out lines. Default low configures serial port as single line I/O.	N/A	00
LSB First	1	<6>	Active high indicates serial port access is LSB to MSB format. Default low indicates MSB to LSB format.	N/A	00
REFCLK<4:0>	5	<5:1>	Reference clock multiplier	N/A	00
PD	1	<0>	Enable automatic power down between bursts	N/A	00
MoreGain	1	<7>	This bit adjusts output selection of the CIC filters. Allows user to gain up the output when interpolation rates are not a power of two.	N/A	01
Continuous Mode	1	<6>	Continuous mode operation enabled. Uses Tx enable pin to synchronize I/Q data: 1=I, 0=Q. Operates only in 12-bit parallel word format.	N/A	01
SLEEP	1	<5>	Active high full sleep mode bit.	N/A	01
FSK Mode	1	<4>	Active high FSK mode. DDS cosine data output.	N/A	01
By pass Inverse SINC Filter	1	<3>	Inverse SINC filter bypassed in data path.	N/A	01
BPLL	1	<2>	Bypass the REFCLK PLL	N/A	01
INFMT	2	<1:0>	Input format select bits: 1x - full word mode, 01 - half-word mode, 00 - quarter word mode.	N/A	01
FTW1<31:0>	32	<7:0> <7:0> <7:0> <7:0>	32-bit DDS frequency tuning word	1	05, 04, 03, 02
INT1<5:0>	6	<7:2>	Interpolation rate bits: these bits program the interpolation rate of the first interpolator. Available rates are 1-64.	1	06
SI1	1	<1>	Spectral inversion bit: Active high enables the spectral inversion capability of the AD9856.	1	06
BPHB3	1	<0>	Bypass third half-band filter	1	06
GS1<7:0>	8	<7:0>	AD8320 gain control bits: Sets the AD8320 line driver gain control data to be output at the dedicated control bus.	1	07
FTW2<31:0>	32	<7:0> <7:0> <7:0> <7:0>	32-bit frequency tuning word	2	0B, 0A, 09, 08

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Table III continued. Control Bus Register Definitions.

Bit name	Width	Position	Description	Profile	Address (Hex)
INT2<5:0>	6	<7:2>	Interpolation rate bits: these bits program the interpolation rate of the first interpolator. Available rates are 1-64.	2	0C
SI2	1	<1>	Spectral inversion bit: Active high enables the spectral inversion capability of the AD9856.	2	0C
BPHB3	1	<0>	Bypass third half-band filter	2	0C
GS2<7:0>	8	<7:0>	AD8320 gain control bits: Sets the AD8320 line driver gain control data to be output at the dedicated control bus.	2	0D
FTW3<31:0>	32	<7:0> <7:0> <7:0> <7:0>	32-bit frequency tuning word	3	11, 10, 0F, 0E
INT3<5:0>	6	<7:2>	Interpolation rate bits: these bits program the interpolation rate of the first interpolator. Available rates are 1-64.	3	12
SI3	1	<1>	Spectral inversion bit: Active high enables the spectral inversion capability of the AD9856.	3	12
BPHB3	1	<0>	Bypass third half-band filter	3	12
GS3<7:0>	8	<7:0>	AD8320 gain control bits: Sets the AD8320 line driver gain control data to be output at the dedicated control bus.	3	13
FTW4<31:0>	32	<7:0> <7:0> <7:0> <7:0>	32-bit frequency tuning word	4	17, 16, 15, 14
INT4<5:0>	6	<7:2>	Interpolation rate bits: these bits program the interpolation rate of the first interpolator. Available rates are 1-64.	4	18
SI4	1	<1>	Spectral inversion bit: Active high enables the spectral inversion capability of the AD9856.	4	18
BPHB3	1	<0>	Bypass third half-band filter	4	18
GS4<7:0>	8	<7:0>	AD8320 gain control bits: Sets the AD8320 line driver gain control data to be output at the dedicated control bus.	4	19

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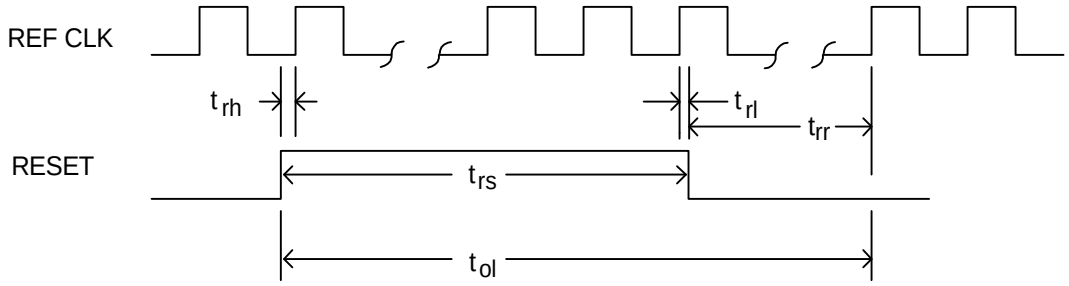
Figure 1. Master Reset Timing Diagram



Symbol	Definition	Min. Spec.
t_{rh}	CLK delay after Reset rising edge	3.5nS
t_{rl}	Reset falling edge after CLK	3.5nS
t_{rs}	Minimum Reset width	5 CLK cycles

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Serial Port Operation

The AD9856 serial control interface is designed to be compatible with most synchronous transfer formats. The interface allows read/write access to all registers that configure the AD9856. Single or multiple byte transfers are supported as well as MSB or LSB transfer formats. The AD9856's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

Communicating with the AD9856 occurs in two phases. The first phase of every communication cycle is the writing of an instruction byte. The second phase is the data transfer as specified by the instruction byte.

Figure 2. Using SDIO as a Read/Write Transfer

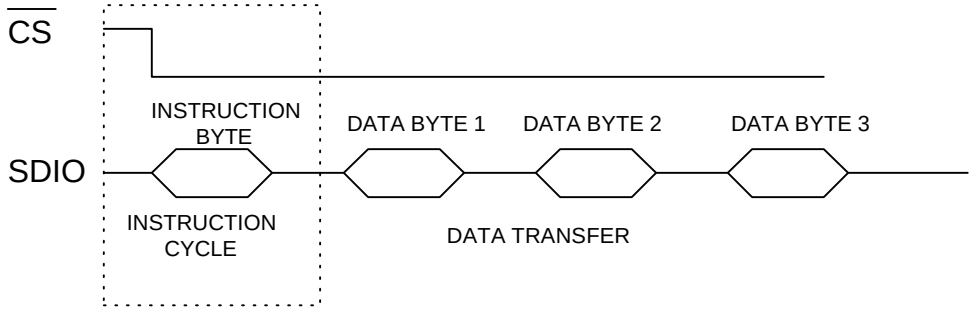
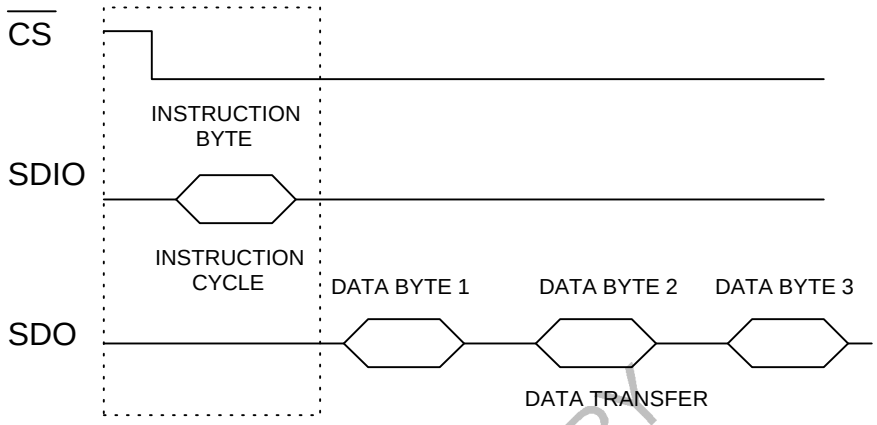


Figure 3. Using SDIO as an Input, SDO as an Output



All data input to the AD9856 is registered on the rising edge of SCLK. All data is driven out of the AD9856 on the falling edge of SCLK.

The instruction byte contains the following information as shown below (see Table IV):

MSB LSB

R/W(Bar)	N1	N0	A4	A3	A2	A1	A0

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R/W (Bar) - Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation.

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N1, N2 - Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle of the communications cycle.

A4, A3, A2, a1, A0 - Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multi-byte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9856. See the MSB/LSB transfer section for details.

Table IV

N1	N0	Description
0	0	transfer 1 byte
0	1	transfer 2 bytes
1	0	transfer 3 bytes
1	1	transfer 4 bytes

PRELIMINARY TECHNICAL DATA

Serial Interface Port Pin Description

The AD9856 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. The serial port can be configured as either a 2-wire or 3-wire hardware interface. The 2-wire operation performs read/write operations on the SDIO pin.
The 3-wire operation performs writes on SDIO and reads data out on the SDO pin.

Definition of serial interface port pins:

SCLK - Serial Clock. The serial clock pin is used to synchronize data to and from the AD9856 and to run the internal state machines. SCLK maximum frequency is 5 MHz.

CS(Bar) - Chip Select (Bar). Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until CS is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO - Serial Data I/O. Data is always written into the AD9856 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by the REG0<7> bit. REG0<7> defaults to logic zero, which configures the SDIO pin as bidirectional.

SDO - Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9856 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

CA CLK - Output clock pin to the AD8320. If using the AD8320 programmable cable driver amplifier and desire the AD9856 to program its gain control register, connect this pin to the CLK input of the AD8320. See the Writing the AD8320 Gain Control Register section for details.

CA Data - Output data pin to the AD8320. If using the AD8320 programmable cable driver amplifier and desire the AD9856 to program its gain control register, connect this pin to the SDATA input of the AD8320. See the Writing the AD8320 Gain Control Register section for details.

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CA Enable - Output Enable pin to the AD8320. If using the AD8320 programmable cable driver amplifier and desire the AD9856 to program its gain control register, connect this pin to the DATAEN input of the AD8320. See the Writing the AD8320 Gain Control Register section for details.

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9856. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9856, coincident with the first 8 SCLK rising edges. The instruction byte provides the AD9856 serial port controller with information regarding the data transfer cycle, which is phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer (1-4), and the starting register address for the first byte of the data transfer as previously shown.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9856. The remaining SCLK edges are for phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9856 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one communication cycle in a multi-byte transfer is the preferred method. However, single byte communication cycles are useful to reduce CPU overhead when register access requires one byte only. Examples of this may be to write the AD9856 SLEEP bit, or an AD8320 gain control byte.

At the completion o any communication cycle, the AD9856 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle. An example of a proper data transfer with the

AD9856 is as follows: From initialization, the AD9856 serial port controller expects the first 8 rising SCLK edges to synchronously write an instruction byte into the AD9856.

PRELIMINARY TECHNICAL DATA

Notes on Serial Port Operation

The AD9856 serial port configuration bits reside in the REG0<7:6> bits. It is important to note that the configuration changes IMMEDIATELY upon writing this register. Writing this register may occur during the middle of a communication cycle.

The AD9856 serial port controller address can roll from 19h to 0h for certain instruction bytes if the MSB first mode is active. The serial port controller address can roll from 0h to 19h for certain instruction bytes if LSB first mode is active.

The system must maintain synchronization with the AD9856 or the internal control logic will not be able to recognize further instructions. For example, if the system sends an instruction byte for a two byte write then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9856 but the next 8 rising SCLK edges are interpreted as the next instruction byte, NOT the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9856, the SYNC I/O pin provides a means to re-establish synchronization without re-initializing the entire chip. The SYNC I/O pin enables the user to reset the AD9856 state machine to accept the next eight (8) SCLK rising edges to be coincident with the instruction phase of a new communication cycle. By applying a “high” signal to the SYNC I/O pin, the AD9856 is set to once more begin performing the communication cycle in synchronization with the system. Any information that had been written to the AD9856 registers during a valid communication cycle prior to loss of synchronization will remain intact.

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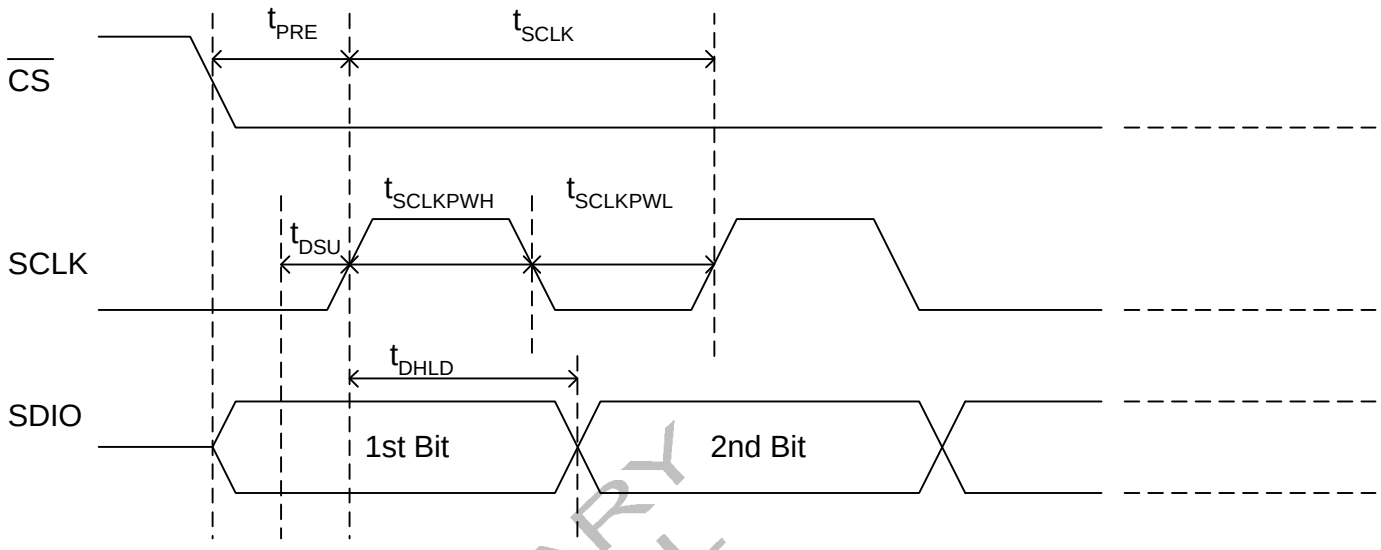
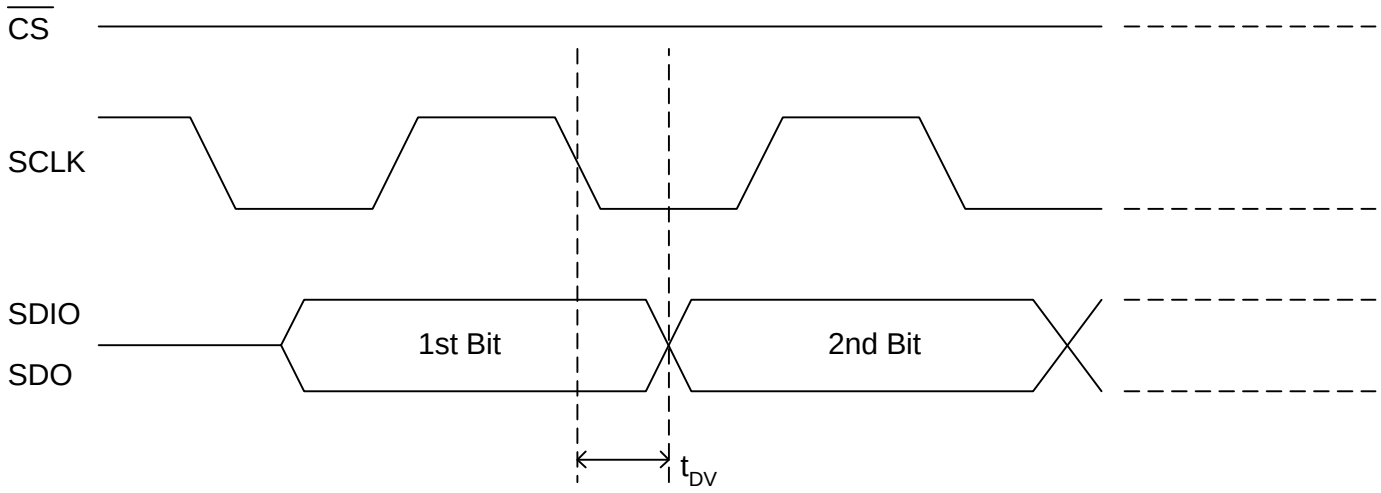
Figure 4. Timing Diagram for Data Write to AD9856



SYMBOL	DEFINITION	MIN SPEC
t_{PRE}	CS to Data Set up Time	30 nS
t_{SCLK}	Period of Serial Data Clock	200 nS
t_{DSU}	Serial Data Set up Time	30 nS
$t_{SCLKPWH}$	Serial Data Clock Pulse Width High	80 nS
$t_{SCLKPWL}$	Serial Data Clock Pulse Width Low	80 nS
t_{DHLD}	Serial Data Hold Time	0 nS

PRELIMINARY TECHNICAL DATA

Figure 5. Timing Diagram for Read from AD9856



SYMBOL	DEFINITION	MIN SPEC
t_{DV}	Data Valid Time	30 nS

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Figure 6. DATA WRITE CYCLE, SCLK IDLE HIGH

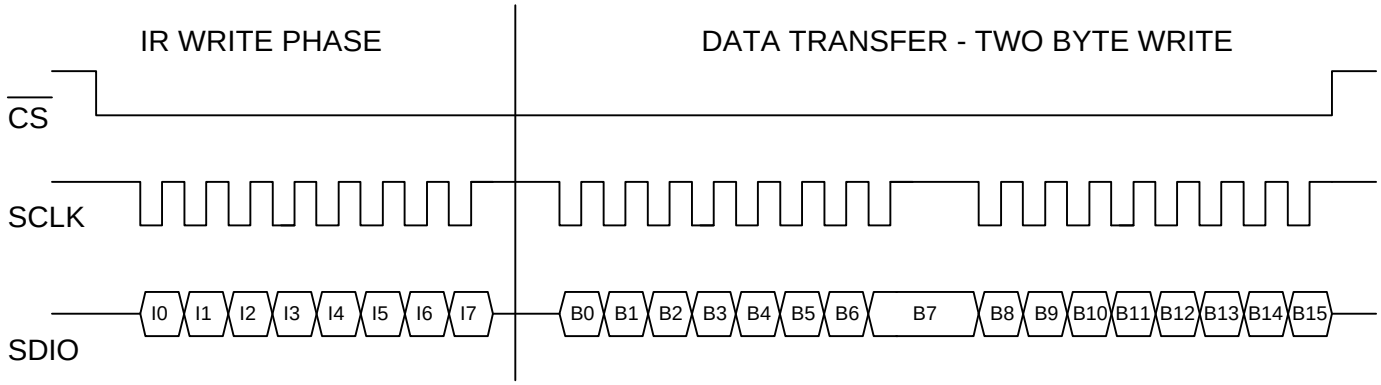
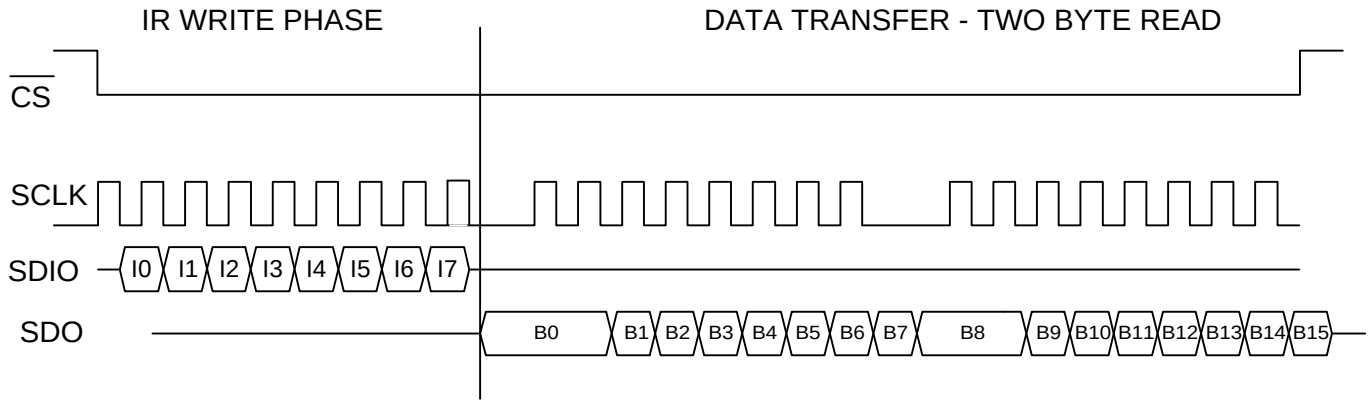


Figure 7. Data read cycle, 3-wire configuration, SCLK IDLE Low



MSB/LSB Transfers

The AD9856 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the REG0<6> bit. When REG0<6> is set active high, the AD9856 serial port is in LSB first format. REG0<6> defaults low, to the MSB first format. The instruction byte must be written in the format indicated by REG0<6>. That is, if the AD9856 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

Multi-byte data transfers in MSB format can be completed by writing an instruction byte which includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multi-byte communication cycle. Multi-byte data transfers in LSB first format can be completed by writing an instruction byte which includes the register address of the least significant byte. In LSB first

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mode, the serial port internal byte address generator increments for each byte required of the multi-byte communication cycle.

Programming/Writing the AD8320 Cable Driver Amplifier Gain Control

Programming the Gain Control register of the AD8320 programmable cable driver amplifier can be accomplished via the AD9856 serial port. Four 8-bit registers (one per profile) within the AD9856 store the gain value to be written to the AD8320. The AD8320 is written via three dedicated AD9856 output pins that are directly connected to the AD8320's serial input port. The transfer of data from the AD9856 to the AD8320 will occur upon detection of three conditions. Each is described below:

1. **Power-up Reset** - The AD9856, upon initial power-up, will write the AD8320 gain control register to all zeros (minimum gain).
2. **Change in profile selection bits (PS1, PS0)** - The AD9856 samples the PS1, PS0 input pins and writes the AD8320 gain control register when a change in profile is determined. The data written to the AD8320 comes from the gain control register associated with the current profile.
3. **Serial port write of AD9856 registers that contain AD8320 data** - The AD9856 will write the AD8320 with data from the gain control register associated with the current profile whenever ANY AD9856 gain control register is written to. The user does not have to write the AD9856 in any particular order or be concerned with time between writes. If the AD9856 is currently writing the AD8320 while one of the four AD9856 gain control registers is being written, the AD9856 will immediately terminate the AD8320 write sequence (without updating the AD8320) and begin a new AD8320 write sequence.

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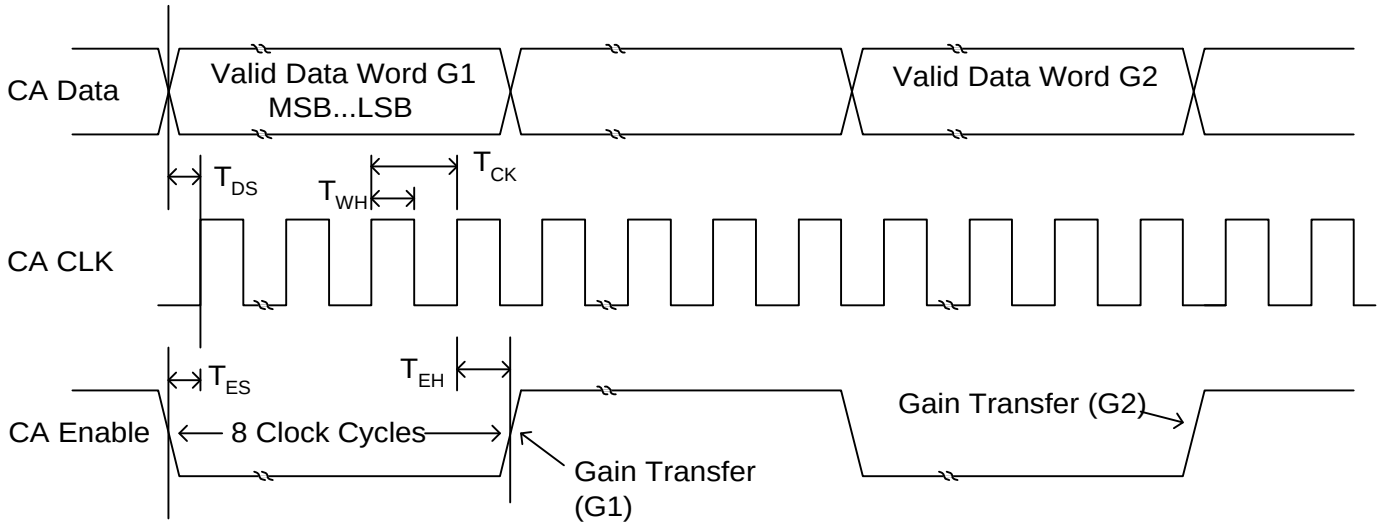
Figure 8. Programmable Cable Driver Amplifier Output Control Interface Timing



Symbol	Definition	Min. Spec.
T_{ds}	CA Data Setup Time	6.5 nS
T_{dh}	CA Data Hold Time	2 nS
t_{wh}	Clock Pulse High	9 nS
t_{ck}	Clock Period	25 nS
t_{es}	CA Enable Setup Time	17 nS
t_{eh}	CA Enable Hold Time	2.0 nS

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Input Formatter - Clock Domains

The AD9856 contains programmable phase-locked loop circuitry that multiplies up the external reference clock frequency input (REFCLK) by integer values, programmable from 4 to 20, to generate the internal reference clock frequency (Fmax). The maximum internal clock frequency is 180 MHz. All other internal clock domains are generated from Fmax. Separate clock domains exist for the Halfband filters and input format logic.

Equations 1-5 relate the clock domains to REFCLK for profiles that do not bypass the third Halfband filter. MULT is the programmable 5-bit register value. INTERPRATE is the current interpolation rate of the CIC filter as selected by the profile bits.

$$Fmax = REFCLK*MULT=F5 \quad \text{(EQ. 1)}$$
$$F4 = (REFCLK*MULT)/INTERPRATE \quad \text{(EQ. 2)}$$
$$F3 = F4/2 = (REFCLK*MULT)/(INTERPRATE*2) \quad \text{(EQ. 3)}$$
$$F2 = F3/2= (REFCLK*MULT)/(INTERPRATE*4) \quad \text{(EQ. 4)}$$
$$F1 = F2/2=(REFCLK*MULT)/(INTERPRATE*8) \quad \text{(EQ. 5)}$$

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The input data format data rate is a function of the Fmax clock rate and the input format mode chosen via the REG1<1:0> bits. If the REG1<1:0> bit is programmed to "1X", the input format selected is a 12-bit word (full word mode). For burst operation, in full word mode, the input timing diagram is shown in figure 9. The data rate, related to Fmax, is given in equation 6.

$$Fin = F2 = (REFCLK*MULT)/(INTERPRATE*4) \quad \text{(EQ. 6)}$$

If the REG1<1:0> bits are programmed to 01, the input format selected is a 6-bit word (half word mode). For burst mode operation in half word mode, the input timing diagram is shown below in figure 10. The data rate, related to Fmax is given by equation 7.

$$Fin = F3 = (REFCLK*MULT)/(INTERPRATE*2) \quad \text{(EQ. 7)}$$

If the REG1<1:0> bits are programmed to 00, the input format selected is a 3-bit word (quarter mode). For burst mode operation in quarter word mode, the input timing diagram is shown below in figure 11. The data rate, related to Fmax, is given by equation 8.

$$Fin = F4 = (REFCLK*MULT)/INTERPRATE \quad \text{(EQ. 8)}$$

I/Q Data Synchronization

The AD9856 accepts I/Q data pairs in 2's complement numbering system, in three different word length modes. For all input format modes, the AD9856 input formatter logic outputs to the data path circuitry, parallel 12-bit I/Q pairs at the data rate F1, as given in equation 5 above. If the BPHB3 filter is set, the parallel 12-bit I/Q pairs are output at F2 as described in equation 4.

Programmable input format modes are: 12-bit, 6-bit, or 3-bit, in Burst Mode operation. In Continuous Mode operation, only the 12-bit input format is accepted.

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12-bit Input Format

Figures 9-11 show the timing relationship between TxEnable and D<11:0> inputs. Note that the AD9856 expects the 12-bit I data followed by the 12-bit Q data. I and Q are 2's complement numbers, the sign bit is D<11> in notation I<11:0>, Q<11:0>.

Figure 9. 12-bit I/Q Input Word Format Diagram

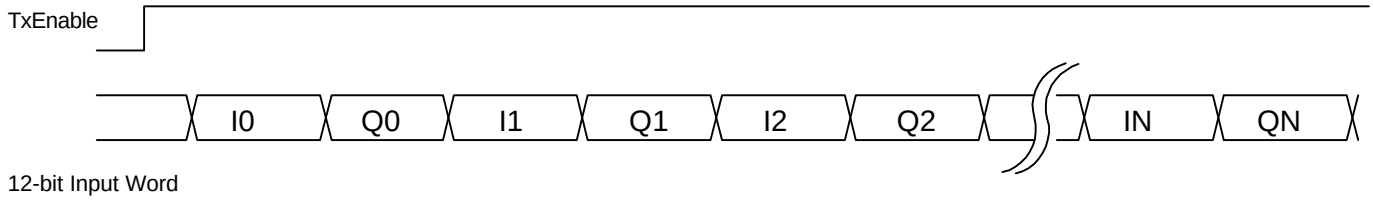


Figure 10. 6-bit I/O Input Word Format Diagram

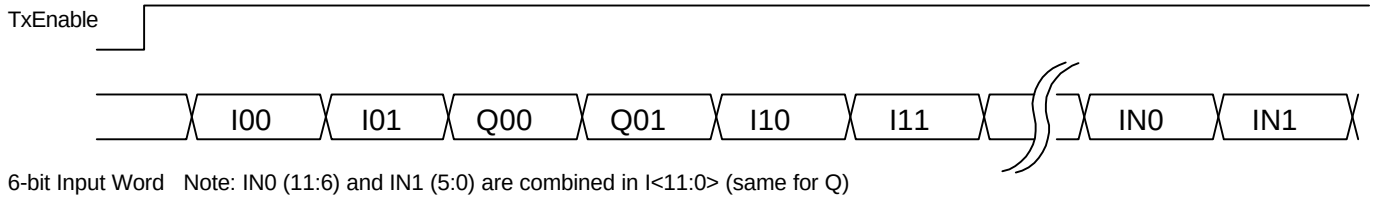
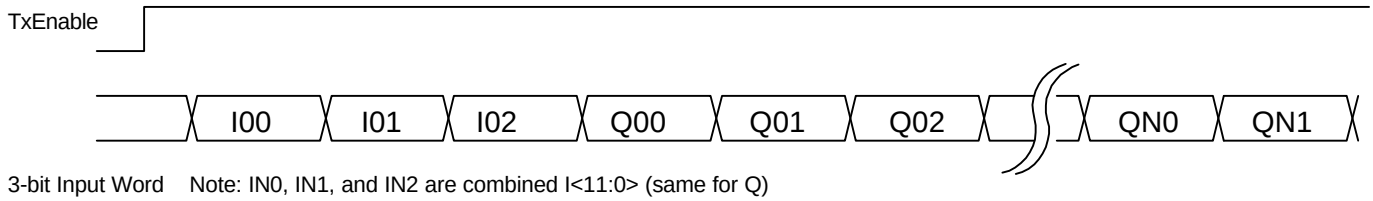


Figure 11. 3-bit I/O Input Word Format Diagram



The AD9856 actually uses the Fmax clock rate to sample the D<11:0> inputs. The user only has to provide data, at the proper data rate, synchronous to the rising edge of TxEnable. The data rate change from Fmax to F1 occurs approximately in the middle of each I/Q input period. (See timing diagram in figure 12 below).

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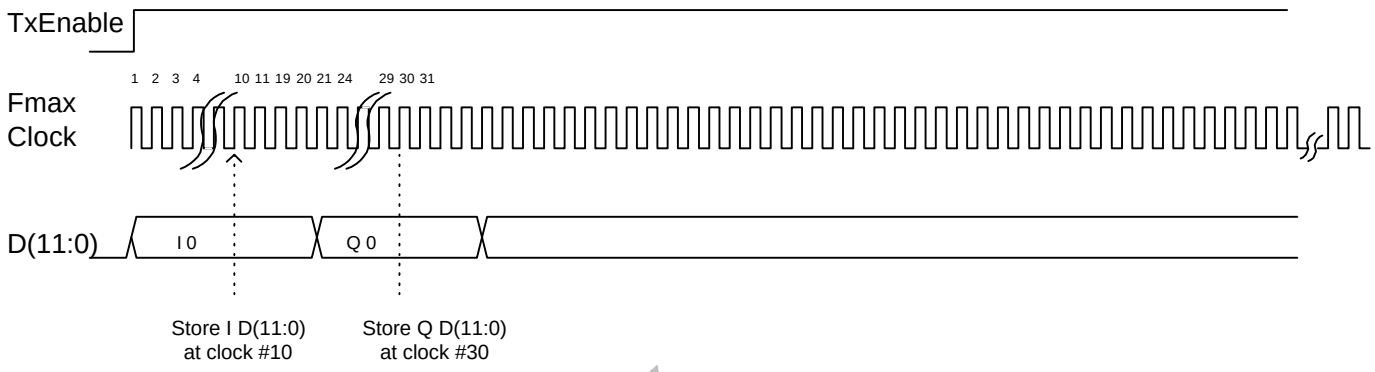
Figure 12. Input I/Q Data Sampling Scheme (12-bit Full Word Mode, interpolation = 5, no halfband filter bypass)



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Determing the I/Q input sample point for the above setup conditions:

For: REFCLK =10 MHz
MULT = 18
INTERP = 5

Fmax = 180 MHz
F4 = 180/5 = 36 MHz
F3 = 36/2 = 18 MHz
F2= 18/2 = 9 MHz
F1 = 4.5 MHz
Fin = 9.0 MHz

The I/Q data period = 180 MHz/9.0 MHz = 20 Fmax clock cycles

Conditions for Maximum Input Data Sampling Rate

The following would be the conditions for achieving the maximum input data sampling rate with the AD9856 device:

12-bit parallel input mode
REFCLK = 10 MHz
MULT = 18
Fmax = 180 MHz
Interp rate = 2 (Halfband3 is bypassed)

In this case,
halfband2 out rate is 90 MHz
halfband1 out rate is 45 MHz
the formatted parallel I/Q rate is 22.5 MHz
the sample rate at the input of the AD9856 is 45 MHz

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Understanding and Using Pin Selectable Modulator Profiles

The AD9856 Quadrature Digital Upconverter is capable of storing four pre-configured modulation modes called "profiles" that define the following:

- Output frequency - 32-bits (register names: FTW1, FTW2, FTW3, FTW4)
- Interpolation rate - 6 bits (bit names: INT1, INT2, INT3, INT4)
- Spectral inversion status - 1 bit (bit names: SI1, SI2, SI3, SI4)
- Bypass 3rd half-band filter - 1 bit (bit names: BPHB1, BPHB2, BPHB3, BPHB4)
- Gain control of AD8320 - 8 bits (register names: GS1, GS2, GS3, GS4)

Output Frequency: This attribute consists of four 8-bit words loaded into four register addresses to form a 32-bit frequency tuning word (FTW) for each profile. The lowest register address corresponds to the least significant 8-bit word . Ascending addresses correspond to increasingly significant 8-bit words. The output frequency equation is given as: Fout = (FTW*Fclk)/2^32.

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Interpolation Rate: Consists of a 6-bit word representing the allowed interpolation values from 1 to 63. Interpolation is the mechanism used to "up-sample" or multiply the input data rate such that it exactly matches that of the DDS sample rate (Fmax). This implies that the system clock must be an exact multiple of the symbol rate. This 6-bit word represents the 6 MSB's of the eight bits allocated for that address. The remaining two bits contain the spectral inversion status bit and half-band bypass bit (see below).

Spectral Inversion: Consists of a 1-bit word that when at logic 0 the default or "non-inverted" output from the adder is sent to the following stages. A logic 1 will cause the inverted output to be sent to the following stages. The non-inverted output is described as I*Cos(wt) - Q*Sin(wt). The inverted output is described as I*Cos(wt) + Q*Sin(wt). This bit is located adjacent to the LSB at the same address as the interpolation rate (see above).

By-pass Third Half-Band Filter: A 1- bit word located in the LSB position of the same address as the interpolation rate (see above). When this bit is logic 0, the third half-band filter (one of three such filters) is engaged and its inherent 2X interpolation rate is applied. When this bit is logic 1, the third half-band filter is by-passed and the 2X interpolation rate is negated. This allows users to input higher data rates - rates that may be too high for the minimum interpolation rate if all three half-band filters with their inherent 2X interpolation rate are engaged. The overall effect is to reduce minimum interpolation rate from X8 to X4.

AD8320 Gain Control: An 8-bit word that controls the gain of an AD8320 Programmable Gain Amplifier connected to the AD9853 with the 3-bit SPI interface bus. Gain range is from -10 dB (00hex) to +26 dB (FFhex). The gain is linear in V/V/LSB and follows the equation: Av = .316 + .077 x Code. Where "Code" is the decimal equivalent of the 8-bit gain word.

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Profile Selection: After profiles have been loaded into the appropriate registers, the user may select which profile to use with two input pins: **PS1** and **PS0,** pins 14 and 15. Profiles are selected according to the table below.

PS1	PS0	PROFILE
0	0	1
0	1	2
1	0	3
1	1	4

Except while in FSK mode, it is recommended that users disable the TX Enable function by bringing that pin to logic 0 prior to changing from one profile to another and then re-asserting TX Enable afterwards. This assures that any discontinuities resulting from register data transfer are not transmitted up or downstream. Furthermore, changing interpolation rates "mid-stream" may create an unrecoverable digital overflow condition that would interrupt transmission until a Reset and reloading procedure would be completed.

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Figure 13. Basic Implementation of AD9856 Digital Modulator and AD8320 Programmable Cable Driver Amplifier in HFC 5-65 MHz Return-path Application.

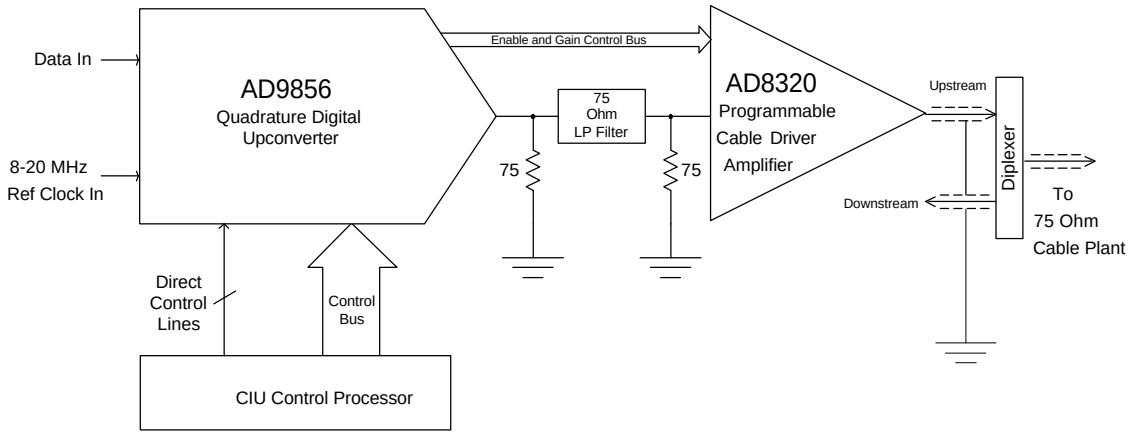
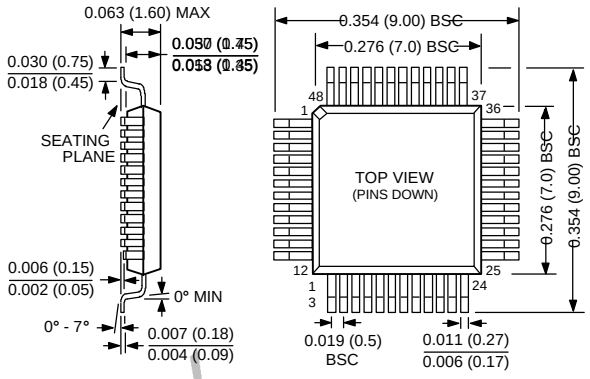


Figure 14. Mechanical Outline
48-Lead Thin Quad Flatpack IC Package (TQFP)



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