SmartFusion Mixed Signal Power Manager

User's Guide

Actel
POWER MATTERS

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Introduction

This document explains how to use the Mixed Signal Power Manager (MPM) reference design for SmartFusion, using the MPM Daughter Card (MPM-DC) connected to either the SmartFusion Evaluation Kit or the SmartFusion Development Kit. You should read the SmartFusion Evaluation Kit User's Guide or the SmartFusion Development Kit User's Guide as appropriate for the configuration you are using with the MPM-DC.

MPM is a reference design that is programmed into a SmartFusion device and can be controlled and modified by the MPM GUI (Graphical User Interface).

Based on Actel's mixed signal flash FPGA technology, MPM delivers superior power monitoring, power sequencing, closed-loop trimming, and power-up and power-down control of up to 22 external power supplies (external regulators). You do not need to use FPGA design tools to configure power management sequencing, levels, or thresholds; the MPM design is programmed into the device through an easy-to-use standalone GUI tool. The GUI enables you to configure power management and drive output signals as the monitored voltages meet or deviate from the user-programmed operating limits, all without opening Actel's Libero® Integrated Design Environment (IDE). This adds more flexibility, reduces total parts count on the board level, and increases system reliability by eliminating single points of failure.

With MPM, use of the Libero tools is optional. Using the MPM GUI tool the user can configure a SmartFusion device that is programmed with the MPM reference design to revise setpoints and change sequencing without opening Libero or reprogramming the FPGA fabric. The MPM GUI tool writes register values to on-chip embedded flash memory, which control power sequencing and monitoring functionality of the MPM reference design.

This document assumes some knowledge of MPM or similar application-specific standard product (ASSP) applications.

System Summary

MPM for SmartFusion

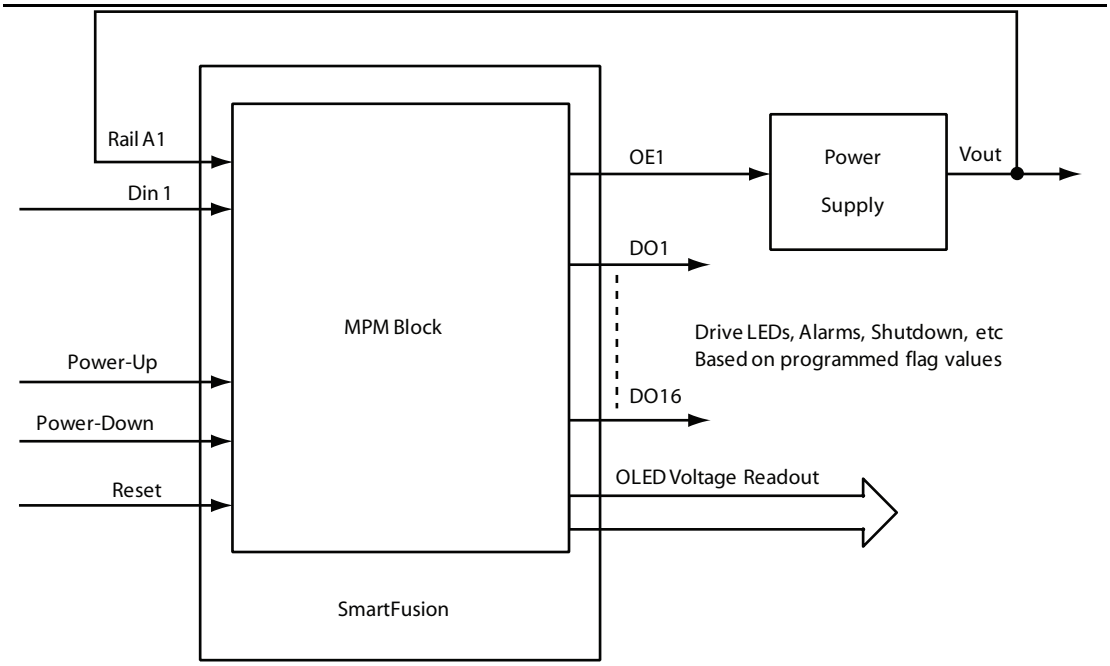

***Figure I-1* • Typical System Level Diagram**

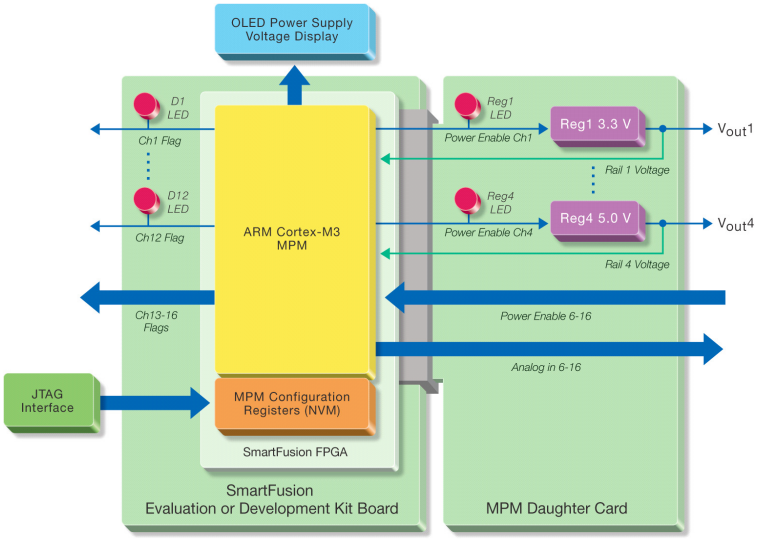

***Figure I-2* • MPM on the MPM Daughter Card (MPM-DC) connected to either the SmartFusion Evaluation Kit or the SmartFusion Development Kit**

Using the MPM GUI, you configure all MPM input and output requirements. You can write to the SmartFusion nonvolatile memory (NVM) using an on-board programmer on the SmartFusion Evaluation Kit or a standard Actel FlashPro4 programmer for the SmartFusion Development Kit via the Joint Test Action Group (JTAG) interface. This sets all threshold flag levels, output signals, power sequencing, and debug level settings for MPM operation. For more information on MPM configuration, refer to "GUI Configuration Tabs". Once programmed, no external functions or connections are required for MPM to function, as it is a standalone application.

When using either the SmartFusion Evaluation Kit or the SmartFusion Development Kit, as a parent board, MPM functionality is demonstrated using the four regulators on the MPM Daughter Card board, which connect to the parent board using the mixed signal header. These four regulators act as independent power supplies that are controlled by MPM.

Output voltages from the on-board regulator power supplies are displayed on the OLED display on the parent board. The OLED is not a required part of an autonomous MPM design. The OLED is used only as part of the reference design for demonstration and debugging purposes.

1 – MPM Graphical User Interface (GUI)

Overview

MPM includes a Windows®-based executable standalone GUI (the MPM GUI) that enables you to access the register data stored in the FPGA NVM. The NVM MPM operation, including voltage limits, digital input and outputs settings, and power sequencing settings, is stored in the NVM within the SmartFusion.

Below are individual sections detailing procedures for using the GUI to install, configure, and run the MPM for SmartFusion designs.

MPM for SmartFusion

Installation

Run the installer and follow the installation wizard instructions. The installer adds Windows Start Menu entries allowing you to run the MPM GUI, browse the design files, and uninstall the package. The MPM GUI also requires that the FlashPro software be installed - you can download FlashPro using the download links on http://www.actel.com/download/program_debug/flashpro/default.aspx.

Using the SmartFusion MPM Demonstration

Having run the installer, you can immediately try out the bundled demonstration program that illustrates some of the features of SmartFusion MPM.

Start by connecting your A2F-EVAL-KIT/A2F-DEV-KIT with your MPM-DC using the respective Mixed-signal headers (J21). To demonstrate open or closed-loop trimming, the following jumpers must be installed on the MPM-DC:

- Regulator trimming circuits: JP12, JP13, JP15, JP14
- Trimming DAC option jumpers. For each of the following, install a jumper on pin 1-2 (On Brd PWM-center): JP19, JP20, JP17, JP18

Connect the 9 V power supply to the MPM daughter card and the USB cables to the parent board.

Note: Two USB connections are required for the A2F-EVAL-KIT board, one for communications and the second to power the board, and as a result there is no power supply connection to the A2F-EVAL-KIT. The A2F-DEV-KIT uses a single USB connection and a separate power supply.

Switch on power for both boards. Now start the MPM GUI by double clicking on the MPM GUI icon or by selecting **Start > Actel SmartFusion MPM Reference Design > MPM GUI**.

Load the demonstration configuration settings by selecting **File > Load Values** and browse to <SF_MPM_RefDesign_Root>\bin\ SF_MPM_Reference_Design.txt.

If this is the first time you have selected **File > Write NVM** or **File > Write NVM & Fabric**, the MPM GUI will prompt you to locate the FlashPro software executable.

If the board has not been programmed with the MPM design previously you need to load the MPM design into the SmartFusion FPGA.

To write the MPM design and all current configuration settings to the SmartFusion device, select **File > Write NVM & Fabric**.

This will write the following design elements to the SmartFusion device on the parent board:

- Fabric logic FDB file
- SmartFusion MSS configuration EFC file
- MPM firmware (stored in an MSS ENVM data storage client by default at ENVM address offset 0x00000000)
- MPM configuration data (stored in an MSS ENVM data storage client by default at ENVN address offset 0x0003F000)

After the MPM design is loaded, you can use **File > Write NVM** to change/update the MPM configuration settings. Once you have programmed the demonstration design and MPM configuration settings the A2F-EVAL-KIT/A2F-DEV-KIT board OLED displays a prompt indicating that the MPM demonstration program is running.

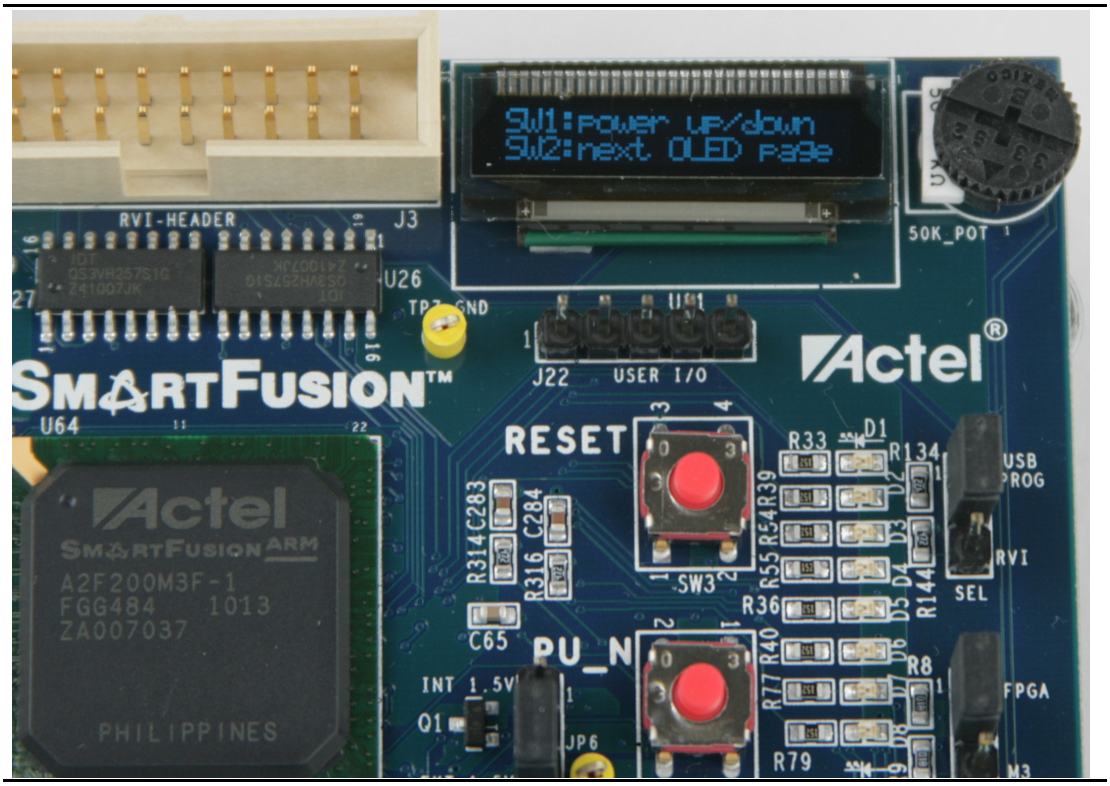

Figure 1-1 • **OLED Message After Successful Programming of the MPM for SmartFusion Reference Design**

Use pushbutton switch SW1 on the parent board to toggle power on and power off sequencing and SW2 to cycle between the various OLED display ‘pages’:

- Help (only displayed once)
- Version (only displayed once)
- MPM status

Table 1 • **MPM Status Description**

Status	Description
Starting	Executing power-on sequencing during which open-loop trimming (if applicable), channel threshold monitoring, and output flag generation are active.
Started	Power sequencing is successful; MPM is now active and reading channel voltages on demand, monitoring channel thresholds, executing closed-loop trimming (if applicable), and generating output flags.

Table 1 • **MPM Status Description**

Status	Description
Stopping	Executing power off sequencing before which closed-loop trimming (if applicable) is switched off but channel threshold monitoring and output flag generation remain operational.
Stopped	Power off sequencing is successful and MPM is idle. None of the following are active – channel threshold monitoring, output flag generation, and open or closed trimming. Channel voltages can be read in any state.

- Channel 1...Channel n voltage and threshold based state (OFF, UV2, UV1, NOM[INAL], OV1, OV2)
- Outputs[15:0] and Outputs[31:16] reflect the current state of the output flags digital output lines where a 1 is represented by a ‘o’ character and a 0 is represented by a ‘.’(For example, 0x1234 = “...o..o...oo.o..”). In the demonstration the following output flags are connected to LEDs:
  - Output 1: MPM-DC LED D0
  - Output 2: MPM-DC LED D1
  - Output 3: MPM-DC LED D2
  - Output 4: MPM-DC LED D3
  - Output 5: MPM-DC LED D4
  - Output 6: MPM-DC LED D5
  - Output 7: MPM-DC LED D6
  - Output 8: MPM-DC LED D7
  - Output 9: A2F-EVAL-KIT/A2F-DEV-KIT LED D1
  - Output 10: A2F-EVAL-KIT/A2F-DEV-KIT LED D2
  - Output 11: A2F-EVAL-KIT/A2F-DEV-KIT LED D3
  - Output 12: A2F-EVAL-KIT/A2F-DEV-KIT LED D4
- Inputs[15:0] and Inputs[31:16] reflect the current state of the general purpose digital inputs which can be combined into the digital output flag generation logic. The same representation of 1 and 0 bits is used as for Outputs[15:0]/[31:16].
- Regulator Enables[15:0] and [31:16] reflect the current state of the regulator enable digital outputs using the same representation as before. In the demonstration design the following regulator enables are connected:
  - Regulator Enable 1: MPM-DC REG1
  - Regulator Enable 2: MPM-DC REG2
  - Regulator Enable 3: MPM-DC REG3
  - Regulator Enable 4: MPM-DC REG4

Using SW2 cycle the OLED display is back to the Status page. Select SW1 to initiate power up sequencing. The state changes to Starting and you can see the various regulator enabled LEDs on the MPM daughter card, turning on. If the status does not change to Started and the power on sequence restarts, then cycle through the individual channels to see which one is not reaching nominal when switched on. Adjust the pot to ensure that it reaches nominal value. If open-loop trimming is enabled, open-loop trim pin voltage will only achieve nominal if the pot is suitably adjusted.

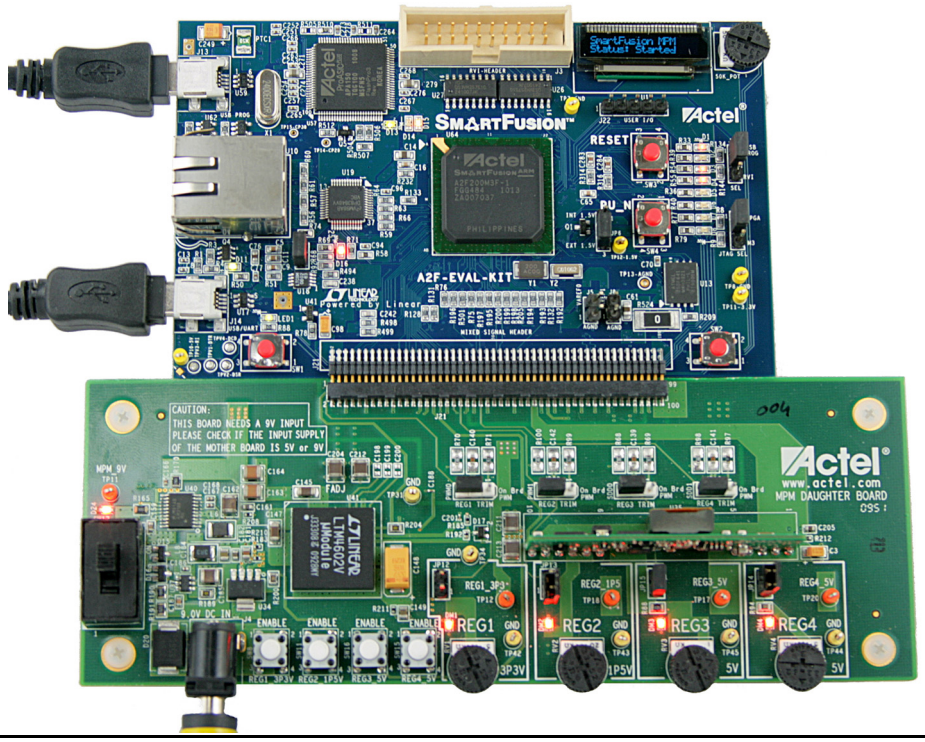

***Figure 1-2* • MPM-DC-KIT MPM Daughter Card Attached to A2F-EVAL-KIT SmartFusion Evaluation Kit**

Once power sequencing has completed and all regulators have reached nominal voltage, the status will change to Started and closed-loop trimming will also be enabled. closed-loop trimming keeps the channel output voltage at the nominal value specified in the GUI even when the pot is adjusted. You can disable trimming by removing the Trim jumper for a given regulator: removing JP12 for regulator 1, JP13 for regulator 2, JP14 for regulator 3, or JP15 for regulator 4 disables closed-loop trimming and you see that the output voltage can be varied using the pot for that channel. Reinstalling the jumper reactivates closed-loop trimming and brings it back to nominal.

Channel A5 is connected to the A2F-EVAL-KIT/A2F-DEV-KIT board RV1 pot controlled 3.3 V circuit and the voltage can be freely adjusted between ~0 V and 2.56 V using the pot. This voltage channel is hard wired to a SmartFusion ACE direct analog input channel which is restricted to a range of 0-2.56 V.

The characteristics of the channels configured in the reference design are as follows:

- Channel A1
  - MPM-DC REG1
  - National Semiconductor LM3100MH 3.3 V nominal regulator
  - Pot range c. 2592-3552 mV
  - ACE ABPS2 +/-5.12 V channel
- Channel A2
  - MPM-DC REG2
  - National Semiconductor LP38693MP-ADJ 1.5 V nominal regulator
  - Pot range c. 1350-1672 mV
  - ACE ABPS6 +/-2.56 V channel

- Channel A3
  - MPM-DC REG3
  - Artesyn ATA010A0X3Z 5 V nominal regulator
  - Pot range c. 3960-5464 mV
  - ACE APBS3 +/- 10.24 V channel
- Channel A4
  - MPM-DC REG4
  - Linear Technologies LTM4602EV 5 V nominal regulator
  - Pot range c. 3832-4928 mV
  - ACE ABPS7 +/- 10.24 V channel
- Channel A5
  - A2F-DEV-KIT/A2F-EVAL-KIT board RV1 circuit
  - 0-3.3 V range
  - Pot range 0-2.56 V
  - ACE ADC Direct Input 0-2.56 V channel

Note: If you use the MPM GUI to configure any of the voltage settings (For example, thresholds +/- hysteresis) out of range of the relevant underlying ACE channel then the MPM firmware will ignore these as invalid and not display them. For example, if you set the OV2 on Channel 5 to 3300 mV then this channel will disappear because even though the RV1 pot on the A2F-EVAL-KIT/A2F-DEV-KIT boards has a range of 0-3.3 V it is hard wired to an ACE direct analog input channel with a range of only 0-2.56 V.

Reference Design Firmware

A SoftConsole workspace containing the reference design firmware and demonstration program application code is included. To access this:

1. Make a backup or work copy of the original SoftConsole workspace.
2. Run SoftConsole v3.1.
3. **File > Switch Workspace > Other…**
4. Browse to the reference design SoftConsole workspace folder - For example, C:\Actel\SF_MPM_RefDesign_v1.0\design_files\SoftConsole_workspace\SF_MPM_RefDesign.
5. Click **OK**.
6. SoftConsole reopens using the reference design firmware workspace that contains a single project implementing the reference design demonstration program.
7. main.c contains the implementation of the reference design demonstration program that interacts with the MPM hardware design through the MPM driver bundled in the project's MPM folder containing mpm.h and mpm.c.
8. Review main.c to see how the MPM driver is used by the demonstration program. Note that the demonstration program also includes other firmware cores used directly by the application code (For example, OLED sample application code built on top of the MSS I2C driver, MSS GPIO driver, MSS Watchdog driver) or by the MPM driver (For example, MSS ACE driver, MSS Timer driver (TIM2), fabric based DirectCore CoreGPIO/CorePWM drivers etc.)
9. mpm/mpm.h describes the public interface to the MPM driver.
10. mpm/mpm.c implements the actual MPM driver functionality that interfaces to the underlying MPM hardware design.

MPM Driver API

The MPM driver API is quite simple and described in the mpm/mpm.h.

```
/* void mpm_init()
 *
 * Initializes the MPM engine "driver" and must be called before any other
 * the other MPM driver methods below.
 */
void mpm_init();

/* void mpm_start()
 *
 * Starts the MPM engine.
 *
 * If MPM is not in state mpm_is_stopped then this method does nothing and
 * just returns immediately otherwise if MPM is in state mpm_is_stopped
 * then this method:
 *
 * - puts MPM into state mpm_is_starting
 * - starts channel threshold monitoring
 * - starts channel open-loop trimming where applicable
 * - initiates power on sequencing
 * - waits until power on sequencing has successfully completed
 * - starts channel closed-loop trimming where applicable
 * - puts MPM into state mpm_is_running
 * - channel threshold monitoring remains active
 */
void mpm_start();

/* void mpm_stop()
 *
 * Stops the MPM engine
 *
 * If MPM is not in state mpm_is_running then this method does nothing and
 * just returns immediately otherwise if MPM is in state mpm_is_running
 * then this method:
 *
 * - puts MPM into state mpm_is_stoping
 * - stops closed-loop trimming where applicable
 * - initiates power down sequencing
 * - waits until power down sequencing has successfully completed
 * - stops open-loop trimming where applicable
 * - stops channel threshold monitoring
 * - puts MPM into state mpm_is_stopped
 */
void mpm_stop();

/* mpm_state_t mpm_get_state()
 *
 * Returns the state that the MPM engine is currently operating in.
 */
mpm_state_t mpm_get_state();

/* mpm_channel_state_t mpm_get_channel_state(mpm_channel_number_t)
 *
 * Returns the current threshold relative state for the channel
 * identified by the channel number passed in. If the channel number
 * passed in does not refer to a valid channel then
 * mpm_channel_is_off is returned.
 */
mpm_channel_state_t mpm_get_channel_state(mpm_channel_number_t);

/* int32_t mpm_get_channel_voltage_mv(mpm_channel_number_t)
 *
```

```
 * Returns the current channel voltage in mV for the channel identified
 * by the channel number passed in. If the channel number passed in does
 * not refer to a valid channel then 0mV is returned.
 *
 * If MPM is in state mpm_is_stopped then mpm_channel_is_off is returned
 * for all channels.
 */
int32_t mpm_get_channel_voltage_mv(mpm_channel_number_t);

/* bool mpm_is_valid_channel(mpm_channel_number_t)
 *
 * Returns true if the channel identified by the channel number pased in is
 * a valid channel recognized by the MPM engine and false otherwise.
 *
 * For a channel to be valid it must meet the following criteria:
 *
 * - Signal name in ACE configuration must be "MPM_Channel_<n>..." where
 *   <n> is a unique identification number between 1 and min(32,
 *   MPM_MAX_NUMBER_OF_CHANNELS) and "..." can be any other text.
 * - ACE configuration for this channel must include one "UNDER" threshold
 *   flag named "DOWN" and one "OVER" threshold flag named "UP" with any
 *   valid voltage level (the threshold voltage levels are dynamically
 *   adjusted at runtime by the MPM engine)
 * - None of the threshold/hysteresis/nominal voltage values configured
 *   through the MPM GUI is out of range of the underlying ACE (ABPS or
 *   direct analog input) voltage channel.
 */
bool mpm_is_valid_channel(mpm_channel_number_t);

/* uint32_t mpm_get_digital_inputs()
 * uint32_t mpm_get_digital_outputs()
 * uint32_t mpm_get_regulator_enable_outputs()
 *
 * Returns a 32 bit bitmask [31:0] representing the current state of the
 * relevant digital I/Os.
 */
uint32_t mpm_get_digital_inputs();
uint32_t mpm_get_digital_outputs();
uint32_t mpm_get_regulator_enable_outputs();
```

Reference Design Hardware

A Libero project implementing the MPM hardware is included. To access this MPM Libero project:

1. Make a backup or work copy of the original Libero project bundled with the package.
2. Run Libero v9.0 SPC.
3. Browse to the Libero project C:\Actel\SF_MPM_RefDesign_v1.0\design_files\Libero_project\SmartFusion_MPM_Reference_Design.
4. Select SmartFusion_MPM_Reference_Design.prj and select **Open**.
5. If you get any warnings about missing IP cores then make sure to download them from the repository to vault using the Libero catalog.
6. The design comprises a top level SmartDesign that instantiates the SmartFusion MSS and several fabric based peripherals.
   - SmartFusion MSS
     - MPM ACE channel and related configuration.
     - MSS GPIOs used for interfacing to SW1/2 pushbuttons and MPM-DC LEDs.
     - MSS ENVM data storage client placeholders for MPM configuration data and MPM firmware.

- Fabric-based logic
  - CoreAPB3 for interfacing MSS to fabric DirectCore peripherals.
  - CoreGPIO (MPM_GPIO_Digital_IOs) implementing up to 32 general digital inputs and 32 flag digital outputs.
  - CoreGPIO (MPM_GPIO_Regulator_Enables) implementing up to 32 regulator enable digital outputs.
  - CorePWM (MPM_PWM_Trimming_Outputs) implementing up to 16 trimming PWM channels.
  - Other ancillary logic – For example, TRIBUFFs for driving the MPM-DC regulator enable digital outputs.

Note: In the reference design, only some output flag digital outputs are connected (to LEDs) and only some regulator enable digital outputs are connected (to regulator enables).

MPM ACE Configuration

MPM channels are configured in the ACE as follows:

1. Signal name must be prefixed with “MPM_Channel_<n>…” where “…” represents any other text needed to name the ACE channel signal and <n> is a unique MPM channel number between 1 and min (32, MPM_MAX_NUMBER_OF_CHANNELS).
2. One OVER threshold named “UP” and one UNDER thresholds named “DOWN” must be configured. The initial voltage values for these thresholds are not important and can be configured to any valid value. The MPM driver will dynamically reprogram these on the fly when managing the channels. For hysteresis-based thresholds the MPM GUI specified hysteresis value will be used. State filtered (assert/de-assert samples) based thresholds are used as is in the ACE configuration.

Channels meeting these criteria and that are not given “out of range” threshold +/- hysteresis configurations via the MPM GUI will be recognized and managed by the MPM firmware.

Note: While modifying/adapting the reference design if ACE configuration is changed, remember to copy the MSS configurator generated drivers_config/mss_ace folder into your SoftConsole project to ensure that the firmware and hardware are always kept in sync.

Running the MPM for SmartFusion Reference Design Demo

1. Connect your A2F-EVAL-KIT/A2F-DEV-KIT parent board to your MPM Daughter Card
2. Ensure that the following MPM DC jumpers are installed:
   - JP17-JP20: pins 1-2 (On Brd PWM-centre) – in order to ensure that the regulator trimming circuits are connected to the fabric based CorePWM outputs from the A2F200 (Refer to "MPM for SmartFusion Reference Design Trimming" section on page 25)
   - JP12-JP15: jumpers on all of these in order to enable (where configured) open-loop trimming during power on sequencing and closed-loop trimming thereafter.
3. Plug in the power supply as required, being careful to connect the 9 V power supply to the MPM-DC only. Switch on power to both boards
4. Run the SF MPM reference design installer and click through the wizard
5. Run the MPM GUI (from the installer or from the **Start** menu)
6. Load the demo configuration settings (SF_MPM_Reference_Design.txt) which should be listed at the bottom of the **File** menu.
7. First time around choose **File > Write NVM & Fabric** to program the whole design (fabric logic FDB, MSS configuration EFC, MPM firmware, and configuration data). First time around you will be prompted to locate the FlashPro executable.
8. Thereafter (assuming you don’t change the Libero project or SoftConsole project) you just need to select **File > Write NVM**.

9. All going well you should see the SF MPM reference design come to life on the OLED. The first OLED “page” displayed should tell you that you use SW1 to alternately select power on or off and SW2 to cycle between the different OLED “pages”.
10. The first two OLED “pages” (Help and Version Information) are only displayed once and not again once you have cycled through all OLED “pages”.
11. You can open the bundled SoftConsole project to see what the demo application code main.c looks like. You can also look at the hardware design and the implementation of the MPM engine “driver” in the SoftConsole project.
12. There are a few GUI items that are basically ignored by the current firmware:
    – DAC Type (only fabric-based CorePWM supported at the moment – no ACE SDD/OBD)
    – Trimming Control > Startup Delay
    – Trim High/Low
    – Margin High/Low
13. For open-loop trimming (active during power on sequencing)
    – Type = open-loop
    – Trim Pin Voltage = voltage required by the regulator’s trim pin to achieve the target nominal
    – If Trim Pin Voltage is 0 then Trim High will be used. If that too is 0 then Trim Low will be used. If all are 0 then open-loop trimming will be skipped.
14. For closed-loop trimming (active after power on sequencing has completed)
    – Type=closed-loop.
    – Trim Pin Voltage=voltage required by the regulator’s trim pin to achieve the target nominal (required because closed-loop effectively implies that open-loop during power up is required). As per 15(c) if all open-loop trim pin voltages are 0 then open-loop and therefore closed-loop trimming will be skipped.
    – Nominal = target nominal voltage to be maintained even if pot is turned.
    – If Nominal is 0 then Margin High will be used. If that too is 0 then Margin Low will be used. If all are 0 then closed-loop trimming will be skipped.
    – Note that the range of the pot for REG3 is such that it can put the channel voltage out of range so that closed-loop trimming cannot get it back to nominal.

GUI Configuration Tabs

Power

The **Power** tab (Figure 1-3) is used to assign requirements for each voltage rail to be controlled, such as the nominal voltage, threshold/flag voltages, and power-up/-down sequences. For more information, refer to the side panel help by clicking on the associated boxes.

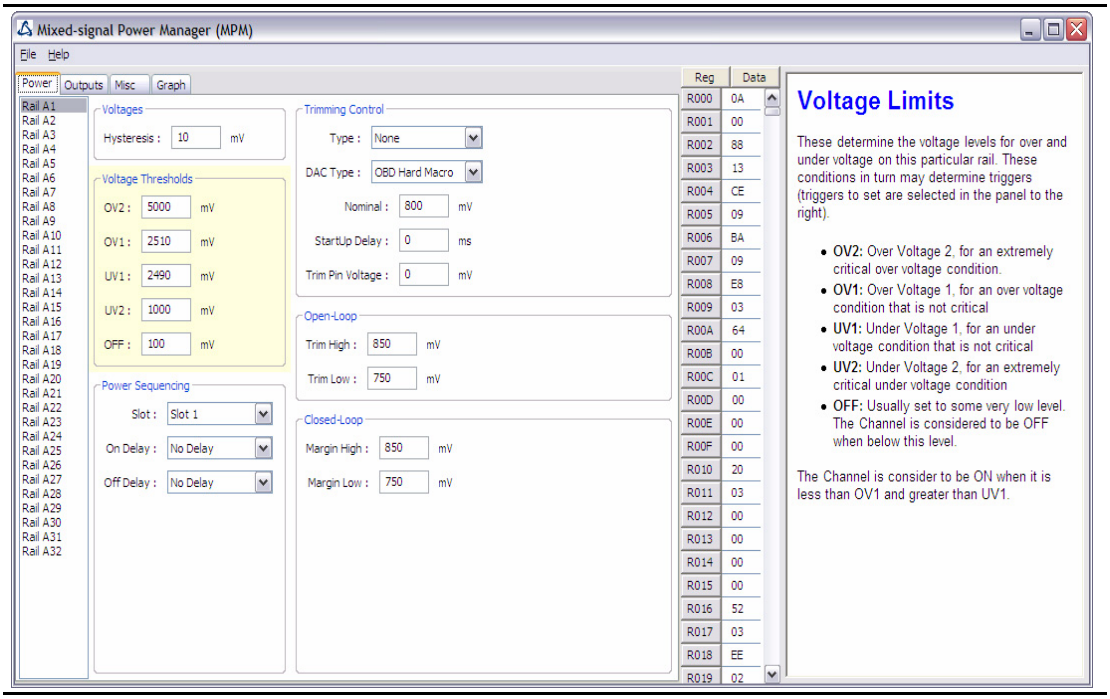

***Figure 1-3* • Power Tab**

Outputs

The **Outputs** tab (Figure 1-4) is used to define the condition for and polarity of the assertion of 16 digital outputs. This tab also enables you to utilize the 16 digital inputs to control the output logic via the digital input panel. For more information, refer to the side panel help by clicking on the associated boxes.

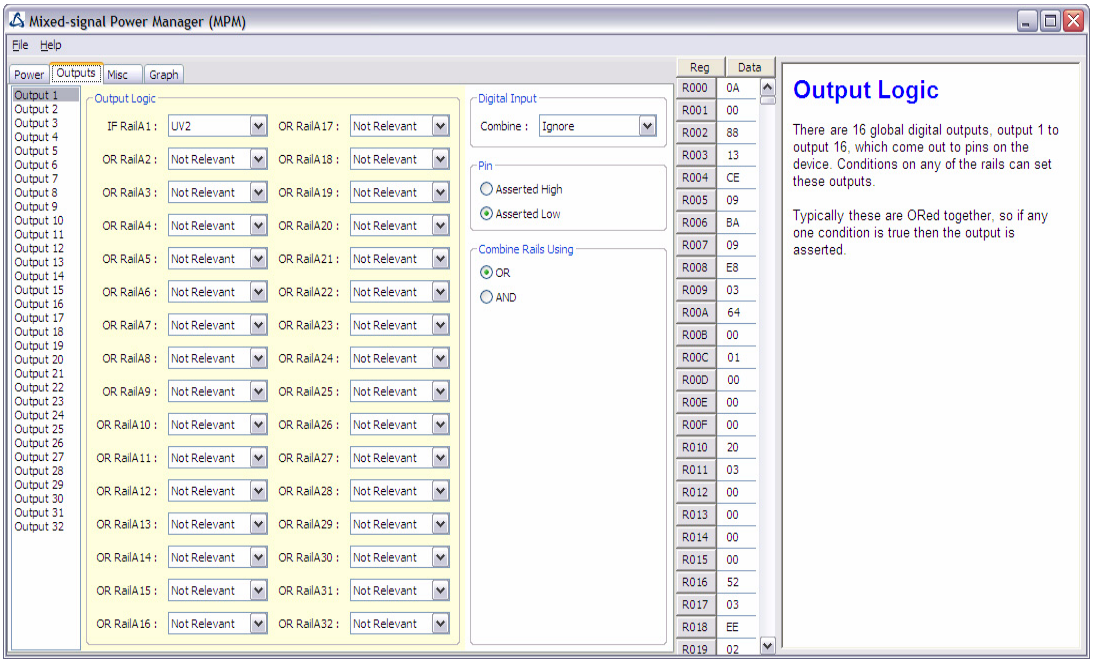

Figure 1-4 • **Outputs Tab**

Misc

The **Misc** tab (Figure 1-5) is used to configure calibration settings and actions on power-up and power-off. For more information, refer to the side panel help by clicking on the associated boxes.

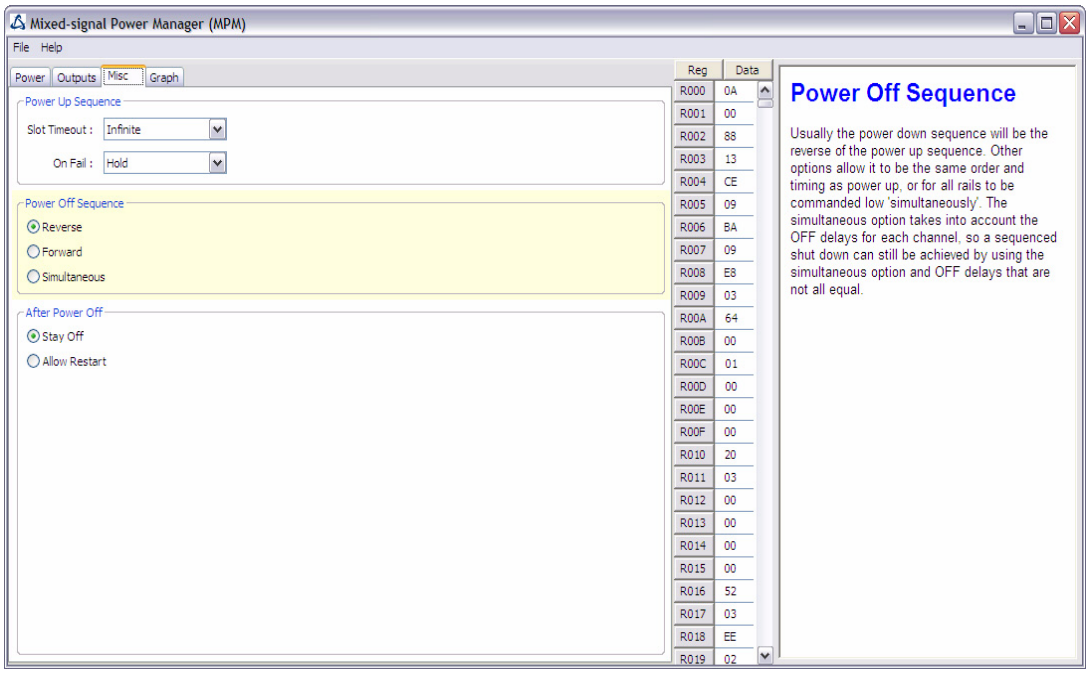

***Figure 1-5* • Misc Tab**

Graph

The **Graph** tab (Figure 1-6) is a visual representation of the power-up and power-down sequencing. It is meant to be used as a visual guideline only, displaying only relative time frames of power-up and power-down as a result of sequencing requirements entered on the **Power** tab. Rise and fall times are not accurate and voltage levels are not taken into account. For more information, refer to the side panel help by clicking on the associated boxes.

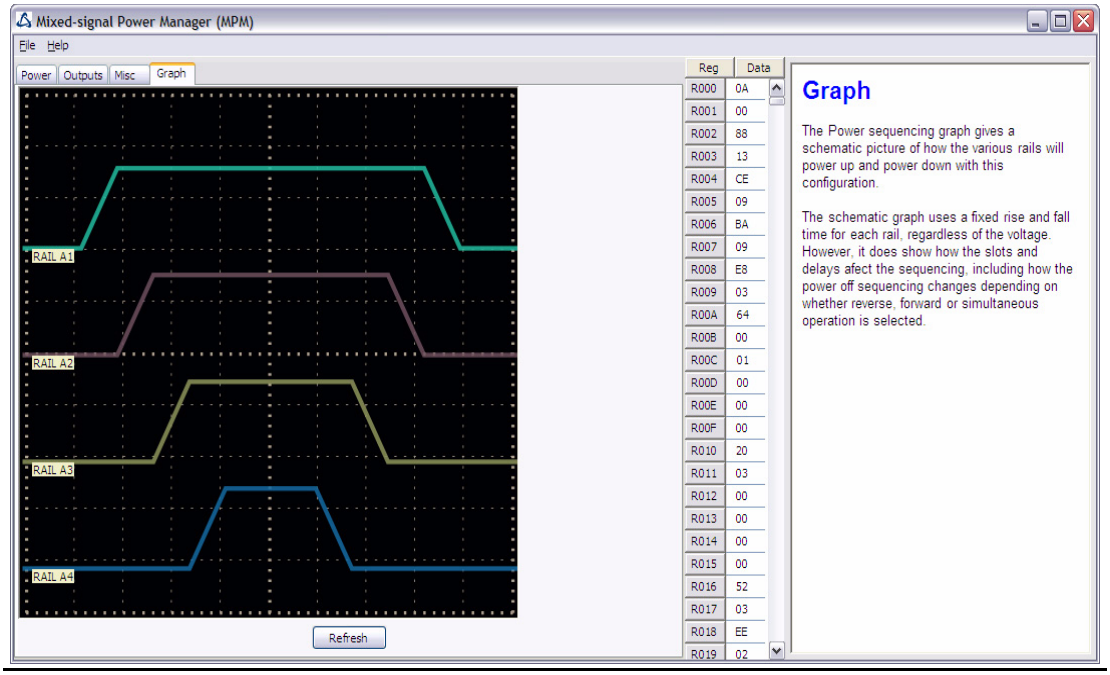

Figure 1-6 • **Graph Tab**

Programming the Device

In the MPM GUI, the column of buttons marked R and followed by a number (Figure 1-7) displays a register map for the configuration data. This relates to how the parameters are stored in the NVM of the FPGA.

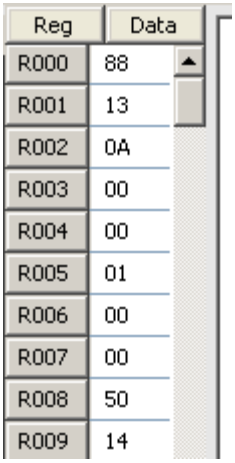

***Figure 1-7* • Register Data**

The **File** menu contains the Write Device and Write NVM menu options.

Write Device programs the NVM register values and the FPGA device with the MPM circuit design. Write Device is required when the FPGA device is either blank or programmed with a different design. You can perform updates to flags and settings using the Write NVM menu option.

Write NVM writes the configuration created using the various tabs in the MPM GUI and programs the register values shown in the column of buttons marked R, followed by a number.

Connections, Jumper Switches, and Settings

Connect jumpers in the default settings to enable the MPM for SmartFusion design to function correctly before powering up the boards.

- Jumpers from FB (feedback voltage) of each regulator for voltage trimming
  - JP12, JP13, JP14, JP15 – Populated with jumper
- Jumpers for selection of PWM or SDD
  - JP17, JP18, JP19, JP20 – Connect pins 1-2
- Push-button switches to disable each regulator and simulate a power failure
  - SW8, SW11, SW15, SW16

Push-button fault injection switches SW8, SW11, SW15, and SW16 ground the enable pin of the corresponding regulator, thereby injecting failure in the power subsystem. However, this enable pin is also connected to the pin on the SmartFusion FPGA (MPM_REG1_EN, MPM_REG2_EN, MPM_REG3_EN, MPM_REG4_EN).The FPGA could be damaged if configured to drive High on the enable line when the fault injection switch is pressed. To avoid this, Actel recommends that the FPGA pin driving this enable should be driving Low or tri-stated.

MPM Reference Design Description

The MPM demonstration design takes advantage of the processing power and programmable flexibility of the SmartFusion™ intelligent mixed signal FPGA on the SmartFusion Evaluation Kit or Development Kit. Connect either kit to the daughter card and download the software as described to run the demo.

The daughter card consists of four regulated power supplies running from a 9 V supply.

- Switching regulator 1.5 V
- Switching regulator 3.3 V
- DC-DC regulator 5 V
- DC-DC regulator 5 V

Using the MPM design one can do the following:

- Monitor voltage for all rails
- Sequence different power rails for power-up and power-down
- Trim and margin a voltage rails in a closed-loop manner
- Sweep the output voltage (POT circuit to change resistor on feedback voltage)
- Induce failures by disabling the enable input of regulator (push-button to GND enable)

Power sequencing is done by sequentially asserting or deasserting channel enable pins for power-up and power-down, respectively, and monitoring the associated channel voltage. All enable pins to the regulator are active high.

Software for MPM Reference Design

Download the MPM Executable that contains the reference design from the Actel website: www.actel.com/products/hardware/devkits_boards/mpm_dc.aspx.

Run the reference design executable. This installs the MPM GUI. From the MPM GUI you can program the demo design into the SmartFusion device and configure your power sequence or trimming. You can update the sequence by uploading only the NVM register locations after the first time you program the main design to the board.

Running the MPM for SmartFusion Reference Design

With the SmartFusion Evaluation Kit

Connect the MPM daughter card to the A2F-EVAL-KIT board. Connect both USB cables from your PC to the evaluation kit. One USB provides power and UART connection; the other provides the programming connection. If you are using the daughter card with the evaluation kit, you can remove the plastic legs and add the rubber feet supplied for this purpose.

With the SmartFusion Development Kit

Connect the MPM daughter card to the A2F-DEV-KIT board. Connect the 9 V power supply to the MPM Daughter Card and the 5 V power supply to the development kit. It is a good idea to double check the voltages before connecting the supplies. Connect the low-cost programming stick to the development kit and connect with a USB cable to the PC for programming. Also connect the other USB cable to the USB connection on the board and to your PC. From the MPM GUI, select File > Write Device to load the MPM design to the device for the first time. Use the switches on the evaluation or development kit to activate the power-up sequence. You can then create interrupts and change POT settings to review the performance of the board. The OLED shows the voltage of each of the first four power rails.

To change the power sequence, use the GUI to change the settings and then do File > Write NVM to update the register settings.

2 – MPM for SmartFusion Reference Design Trimming

Purpose

The purpose of this section is to provide an overview of trimming functionality in the SmartFusion Reference design. This document applies to SmartFusion MPM Reference Design v1.0.

Operation

Overview

In general the purpose of trimming is to perform small adjustments on the output voltage of a regulator or power supply (less than 10% of the output) by driving the trim, adjust, or feedback pin of the regulator. There are two main modes for trimming, open-loop and closed-loop, as described below.

open-loop Trimming

The hardware for open-loop trimming resembles the setup described in Figure 2-1.

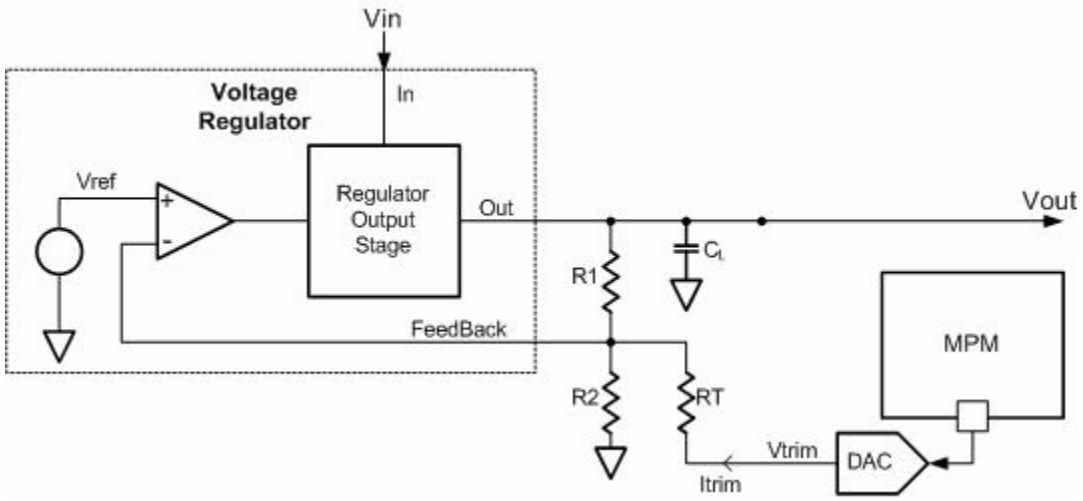

***Figure 2-1* • Open-loop Trimming Using SmartFusion MPM**

The regulator feedback is controlled by SmartFusion MPM, which outputs a pulse-width modulated (PWM) signal that acts as a DAC when fed through a low pass filter such as an RC network. With open-loop trimming, you can adjust the regulator output voltage by driving this signal with different voltages of small variation.

Open-loop trimming is a passive mode. It is not run continually; the feedback pin value is never adjusted. SmartFusion MPM sets the feedback pin value at system initialization and leaves it at that fixed value until a reset or power cycle occurs.

closed-loop Trimming

The hardware for closed-loop trimming is identical to that of open-loop trimming, except that there is feedback from the regulator output to SmartFusion MPM, as seen in Figure 2-2.

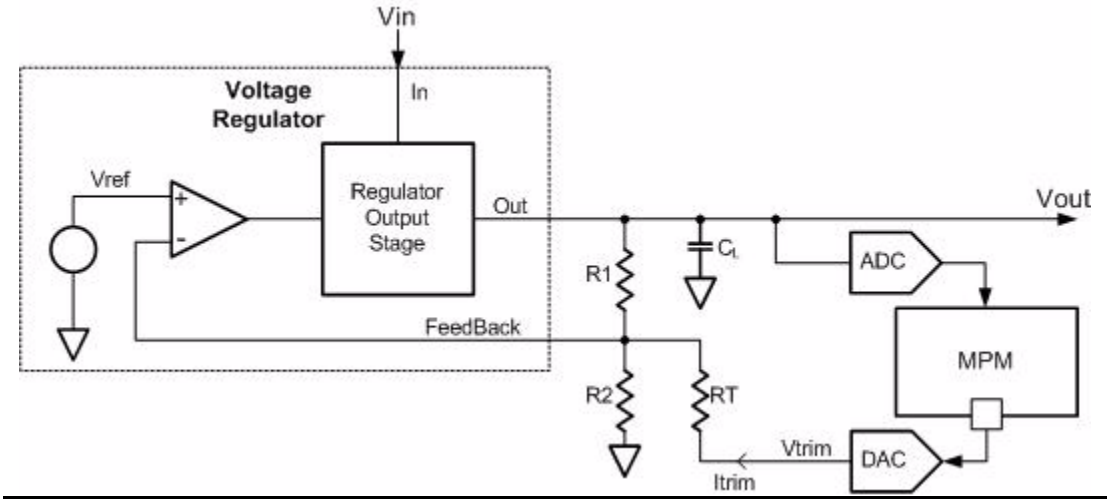

***Figure 2-2* • Closed-loop Trimming Using SmartFusion MPM**

In closed-loop trimming, MPM constantly scans (once per loop) the output voltage of the regulator, and actively adjusts the regulator feedback voltage to drive the regulator to some target output voltage.

Closed-loop trimming is an active mode, it is continually operating. The algorithm for trimming is linear, and is done thus:

1. Read Vout (rail value)
2. Compare Vout to Vouttarget
3. Set Vtrim according to the following:
   - If Vout > Vouttarget, Vtrim = Vtrim + 1
   - If Vout < Vouttarget, Vtrim = Vtrim – 1

Refer to "Type" section on page 27 for how Vouttarget is determined.

Note: For the SmartFusion MPM Reference Design v1.0, the DAC is implemented using CorePWM in low-ripple DAC mode in FPGA fabric and an RC network.

SmartFusion MPM is responsible for driving the Vtrim pin of the above systems (both open-loop and closed-loop). However, varying the RT and R2 resistances (R1 is typically internal to regulators) changes the regulator's sensitivity to variations on the Rtrim pin. It is your responsibility to ensure that RT is big enough so that Vtrim variations will not put the regulator out of its operating range (typically only small variations on the Feedback pin are allowed, on the order of mV), and not so big as to make Vtrim voltages changes negligible to the system.

Suggested resistances, as well as trim pin voltage ranges (typically around 0.8 V) can usually be found in regulator datasheets and associated Application Notes.

GUI Operation

The sections of the GUI highlighted in Figure 2-3 below define configuration parameters used for trimming on a per-channel basis.

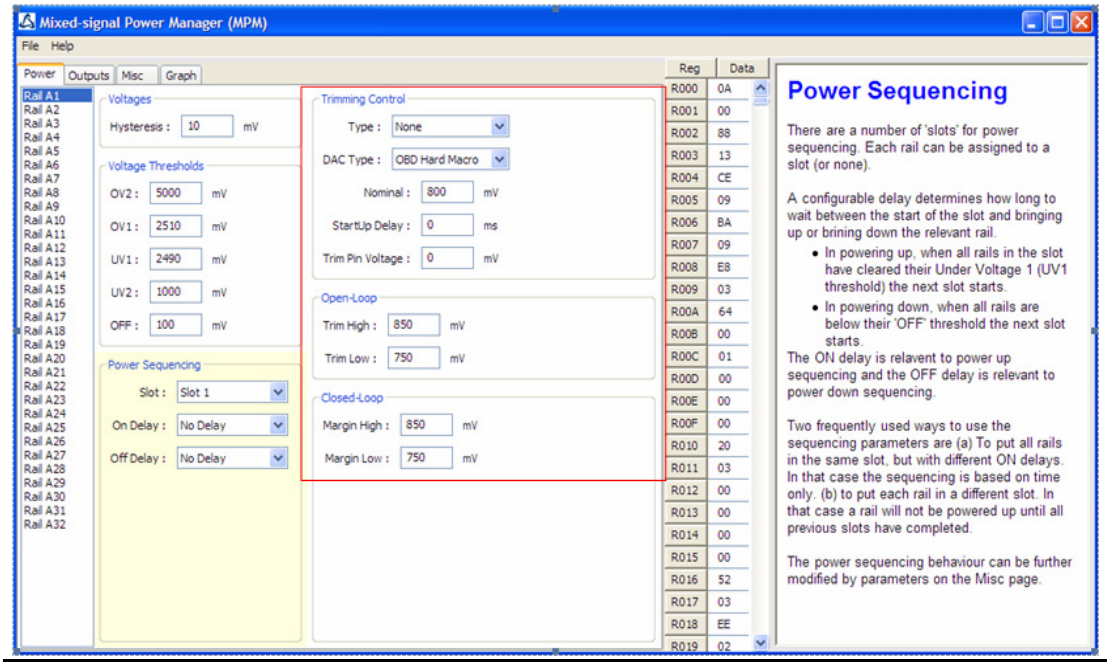

***Figure 2-3* • Trimming GUI Section**

Trimming Control

The following section describes the parameters in the Trimming Control pane of the **Power** tab of the GUI. Clicking on the pane displays online on the right side of the GUI.

Type

This is the trimming type as described in "Operation" section on page 25.

None

Trimming is not performed for this rail. The portion of the MPM loop that would normally be executed for trimming is skipped for this particular rail, and there is no PWM assigned to this rail.

open-loop

On reset, the trim pin is driven with one of three values:

1. Trim Pin Voltage; if that is set to ‘0’, then
2. Trim High; if that is set to ‘0’, then
3. Trim Low

After startup, the trim pin is never adjusted again. The only way to change the level is to reprogram the NVM configuration data.

closed-loop

As with open-loop, on reset the trim pin is driven with one of three values:

1. Trim Pin Voltage; if that is set to ‘0’, then
2. Trim High; if that is set to ‘0’, then
3. Trim Low

However, after all rails have been powered up, the trim pin voltage is adjusted according to the scheme described in "closed-loop Trimming" section on page 26. The target voltage (Vouttarget) is one of three values:

1. Nominal; if that is set to ‘0’, then
2. Margin High; if that is set to ‘0’, then
3. Margin Low.

Note: This is a target voltage, and it is up to you to ensure that the voltage is within the operating range of the system. That is, it is up to you to ensure that the voltage range on the DAC output, which goes from 0 V to 3.3 V, is sufficient for the system (feedback resistor, voltage dividor, trim pin operating range, etc.) and for the amount of trimming expected to be performed.

DAC Type

For trimming, this determines the type of DAC used for this rail.

Note: In SmartFusion MPM v1.0, only the FPGA Fabric option is implemented, so the OBD Hard-Macro is never used.

OBD Hard-Macro

The SmartFusion on-chip Sigma Delta DAC.

FPGA Fabric

CorePWM in low-ripple DAC mode. Requires a low-pass filter at the output of the digital I/O.

Startup Delay

Note: This variable is unused in SmartFusion MPM v1.0.

This determines the amount of time (in ms) MPM should wait, after all rails have powered up during sequencing, before commencing active closed-loop trimming.

3 – MPM Daughter Card Hardware Guide

Introduction

The Mixed signal Power Manager (MPM) Daughter Card enables system designers to evaluate the functionality of Actel's power management solutions in hardware with a four-regulator benchtop power management development system. The MPM daughter card includes four regulators, four voltage bias potentiometers and four fault introduction pushbutton switches, implementing four fully independent power supplies that can be varied and interrupted to demonstrate the management capabilities of Actel's mixed signal power management solution, MPM.

MPM takes advantage of the processing power and programmable flexibility of the SmartFusion™ intelligent mixed signal FPGAs included on the SmartFusion Evaluation Kit or SmartFusion Development Kit when these kits are connected to the MPM daughter card and programmed with the MPM reference design. This section explores the MPM Daughter Card board hardware.

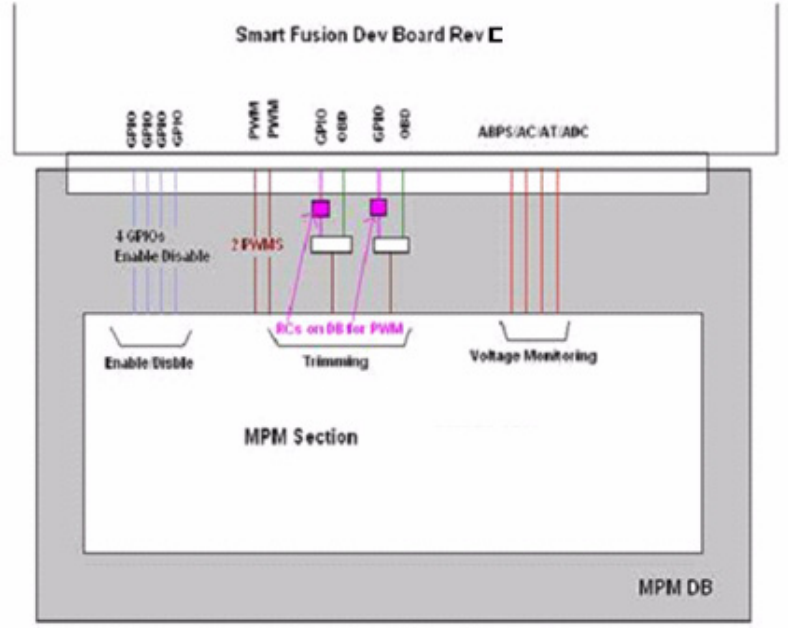

***Figure 3-1* • MPM Daughter Card**

Kit Contents

***Table 1* • MPM Daughter Card Kit Contents**

Quantity	Description
1	MPM Daughter Card
1	9 V power supply
5	Jumpers in small packet
1	Quick Start Card

Web-based Resources

SmartFusion Development Kit

http://www.actel.com/products/hardware/devkits_boards/smartfusion_dev.aspx

SmartFusion Reference Documents

www.actel.com/products/smartfusion/docs.aspx

Libero IDE Design Software

www.actel.com/products/software/libero/default.aspx

Board Description

The MPM Daughter Card provides a benchtop demonstration and development platform for Actel's MPM reference design. MPM delivers power monitoring, power sequencing, and threshold monitoring of up to 22 power regulators using an easy-to-use standalone GUI tool.

Designers using MPM can now replace discrete power management devices, add more flexibility by leveraging SmartFusion's reprogrammable flash FPGA technology, and reduce total parts count at the board level. MPM delivers highly configurable, integrated power management using one high-reliability low-power flash-based SmartFusion mixed signal FPGA.

The MPM daughter board, shown in the figure below, connects to the SmartFusion Evaluation Kit (A2F-EVAL-KIT) or the SmartFusion Development Kit (A2F-DEV-KIT) via the mixed signal header.

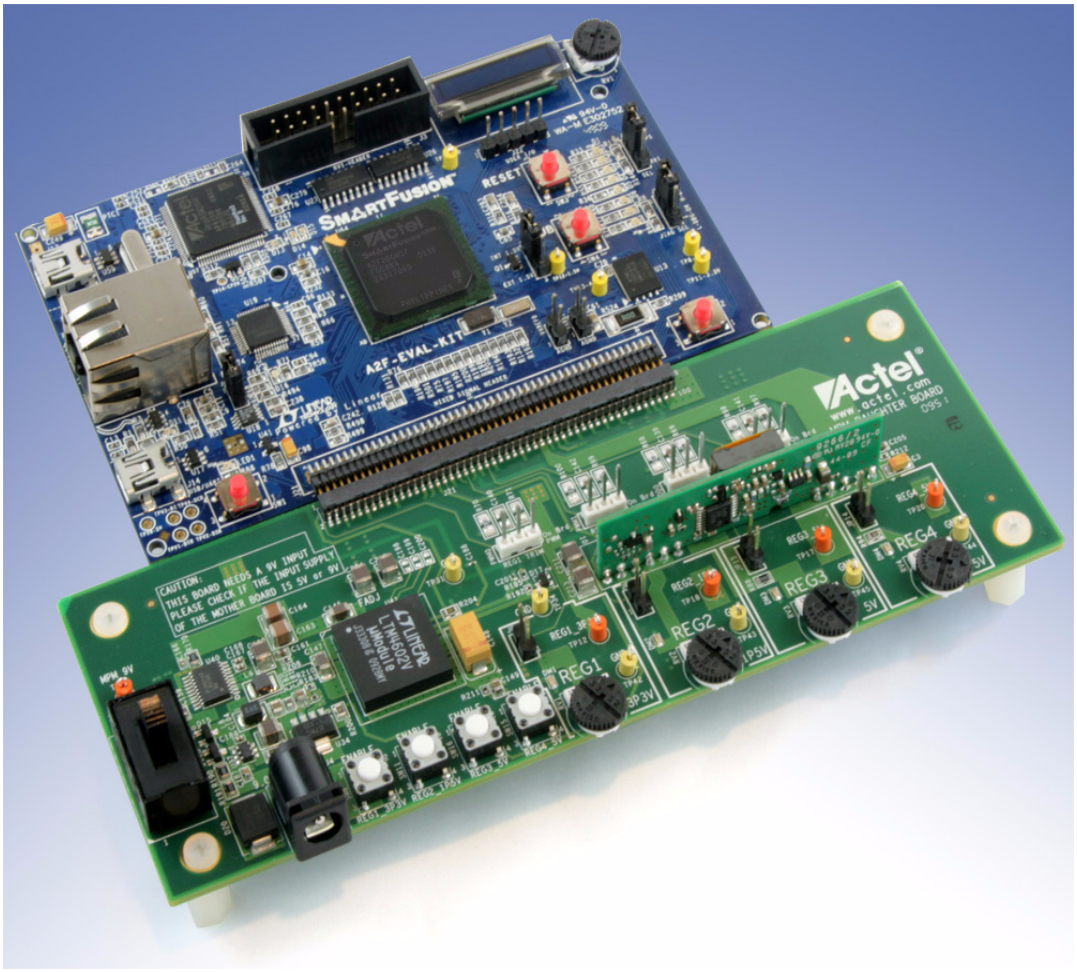

***Figure 3-2* • MPM Daughter Board with SmartFusion Eval Kit**

Mixed Signal Power Manager Board Components

Table 2 • **Mixed Signal Power Manager (MPM) Board Components**

Sl.No.	Name	Description
1	MPM_REG1_5V	5 V Regulated Supply1, Lineage Power ATA010A0X43
2	MPM_REG2_5V	5 V Regulated Supply2, Linear Technology
3	MPM_REG1_3P3	3.3 V Regulated Supply, National LM3100MH
4	MPM_REG2_1P5	1.5 V Regulated Supply, National LP38693-ADJ
5	RV1, RV2, RV3, RV4	POT to vary the voltage O/P of regulator
6	SW8, SW11, SW15, SW16	Switch to Enable/Diable MPM voltage regulators

Installation and Settings

Jumper and Switch Settings

Recommended default jumper settings are defined in Table 3. Connect jumpers in the default settings to enable the pre-programmed reference design to function correctly.

Table 3 • **Jumper Settings (MPM)**

Jumper	Development Kit Function	Default Setting
JP12	Jumper from pin FB (Feedback Voltage) of 3.3 V Regulator for Voltage Trimming	Closed
JP13	Jumper from pin ADJ (Adjust Voltage) of 1.5 V Regulator for Voltage Trimming	Closed
JP14	Jumper from pin Voset (Voltage) of 5 V DC-DC Regulator for Voltage Trimming	Closed
JP15	Jumper from pin Trim (Voltage) of 5 V DC-DC Convertor output for Voltage Trimming	Closed
JP19	Trimming DAC Option Reg1	PWM0
JP20	Trimming DAC Option Reg2	PWM1
JP17	Trimming DAC Option Reg3	SDD0
JP18	Trimming DAC Option Reg4	SDD1

Table 4 • **Table Switches (MPM)**

Switch	Comments
SW17	Switch ON 9 V DC into MPM
SW8	Push-button to disable 3.3 V Supply regulator
SW11	Push-button to disable 1.5 V Supply regulator
SW16	Push-button to disable 5 V Supply regulator (ARTESYN)
SW15	Push-button to disable 5 V Supply regulator (Linear Tech)

Note: The push-button SW8, SW11, SW15, and SW16 grounds the Enable pin of the corresponding regulator, thereby injecting failure in power subsystem. However, this Enable pin is also connected to the pin on FPGA (MPM_REG1_EN, MPM_REG2_EN, MPM_REG3_EN, and MPM_REG4_EN). The FPGA could be damaged if it is driving HIGH on enable line and simultaneously shorted to ground. To avoid this, it is recommended that the FPGA pin driving these enables should be either driving Low or tri_state.

Hardware Components

Mixed Signal Power Management Description

The MPM Daughter Card includes 4 sets of regulated power supply running from a 9 V supply.

- Switching Regulator 1.5 V
- Switching Regulator 3.3 V
- DC-DCRegulators 5 V
- DC-DC Regulators 5 V

Using the MPM GUI you can:

- Monitor voltage for all Rails
- Sequence different Power rails for Power-up and Power-down
- Trim and Margin Voltage Rails in a closed-loop
- Sweep the output voltage (POT circuit to change resistor on feedback voltage)
- Induce failures by disabling the Enable input of regulator (Push button to GND Enable)

MPM manages power sequencing by sequentially asserting or deasserting channel enable pins for power up and power down as per the configuration defined in the MPM GUI and written to on-chip non-volatile memory registers, and monitoring the associated channel voltage. All Enable pins to the regulators are ‘active’ high.

Board Components

3.3 V Supply, MPM_REG1_3P3, National LM3100MH:

This regulated switching mode power supply can deliver up to 1.5 A of output current with regulated output voltage from 0.8 Vdc to 5.0 Vdc over a wide range of input voltage (VIN = 4.5 – 36 V dc). Different output voltages can be set by changing the value of feedback voltage on feedback pin (FB) using resistor feedback divider.

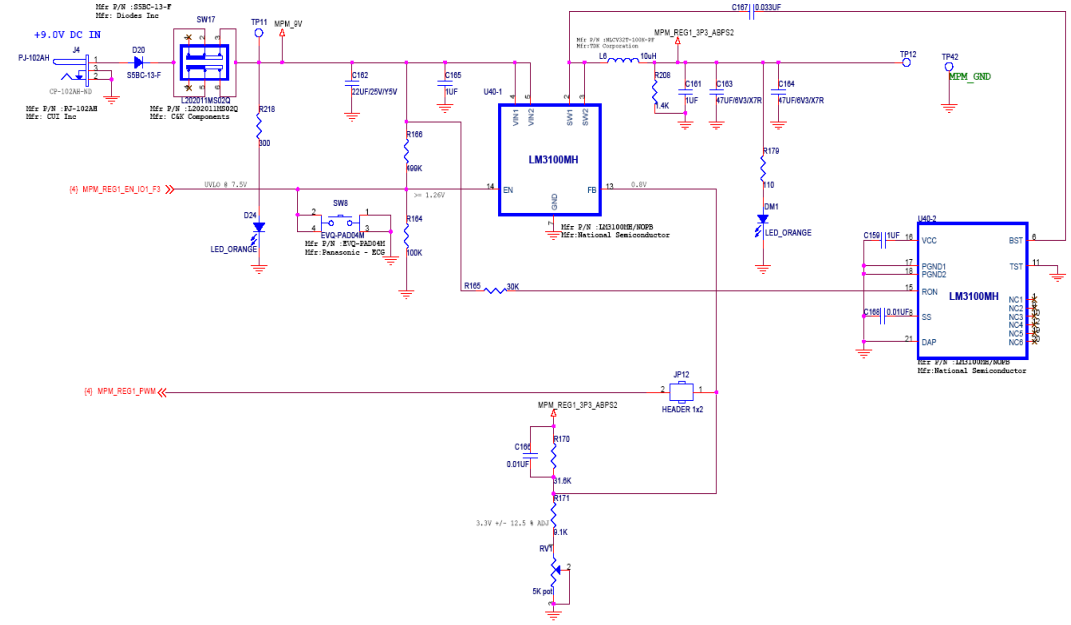

Figure 3-3 **• MPM Switching Power Supply 3.3 V**

1.5 V Power Supply, MPM_REG2_1P5, National LP38693-ADJ

This is Low drop out voltage regulator (250 mv @ 500 ma with 5 V o/p) with output voltage range from 1.25 V to 9 V. The input has a wide input range from 2.7 V to 10 V. The output voltage can be set by controlling the voltage feedback input to ADJ. Pulling the enable pin down to a logic low turns off the part.

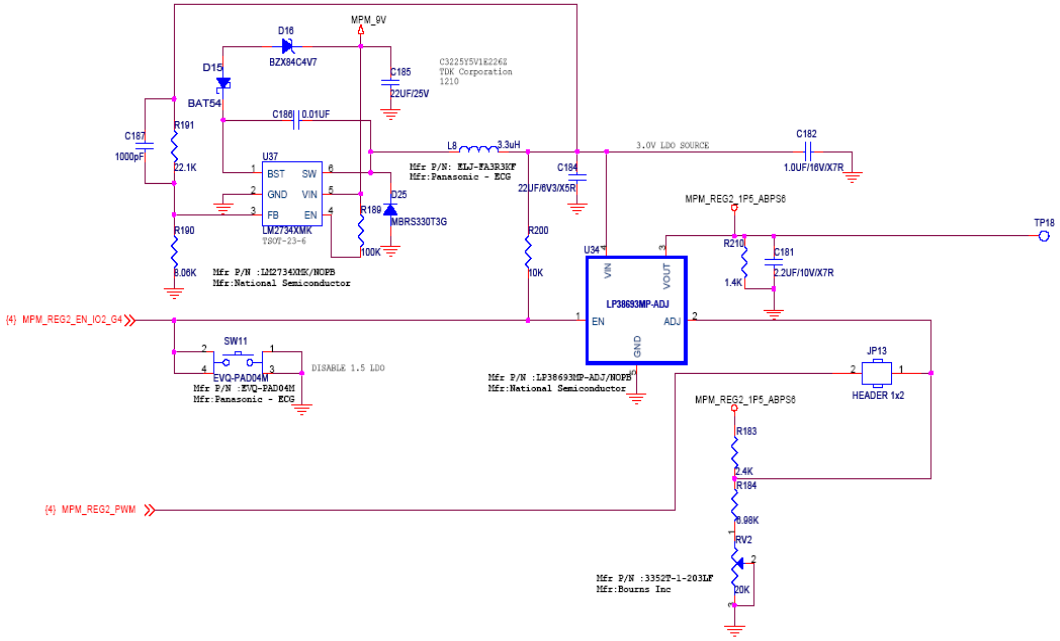

***Figure 3-4* • MPM Switching PowerSupply 1.5 V**

5 V Power supply 1, MPM_REG3_5V, Lineage Power ATA010A0X43

12 V SIP (singe in-line package) power module can deliver up to 10 A of output current with regulated output voltage from 0.75 Vdc to 5.0 Vdc over a wide range of input voltage (VIN = 8.3 – 14 Vdc). The output voltage can be controlled using an external resistor between the TRIM and the GROUND pins of the module.

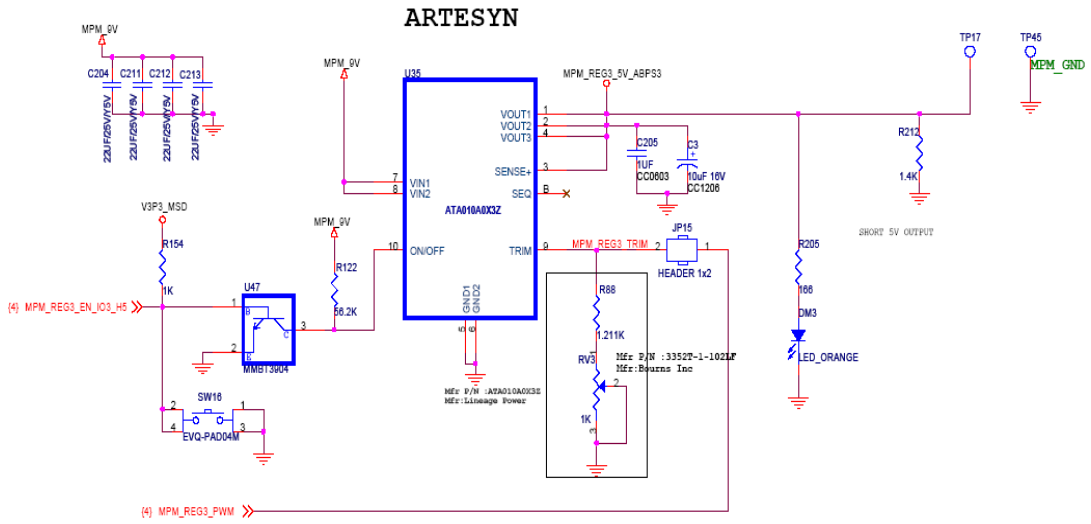

***Figure 3-5* • MPM DC-DC Power Supply 5 V**

5 Volt Supply 2, MPM_REG4_5V, Linear Technology LTM 4602

This DC/DC converter can deliver up to 6A of output current with regulated output voltage from 0.6 Vdc to 5.0 Vdc over a wide range of input voltage (VIN = 4.5 – 20 V dc). Different output voltages can be programmed with using resistors between the VOSET and SGND pins.

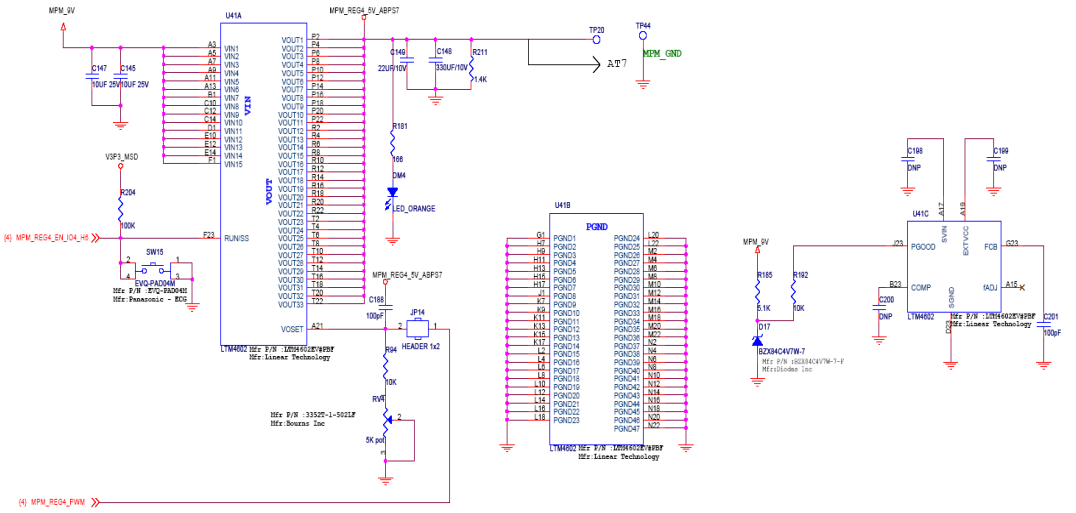

Figure 3-6 • **MPM DC-DC PowerSupply 5 V**

Power

The MPM-DC kit includes an external 9 V Supply.

Connector

MPM Daughter Board Mixed Signal Header for SmartFusion Board

This connector is for interfacing MPM board on to SmartFusion Board Mixed Signal Header.

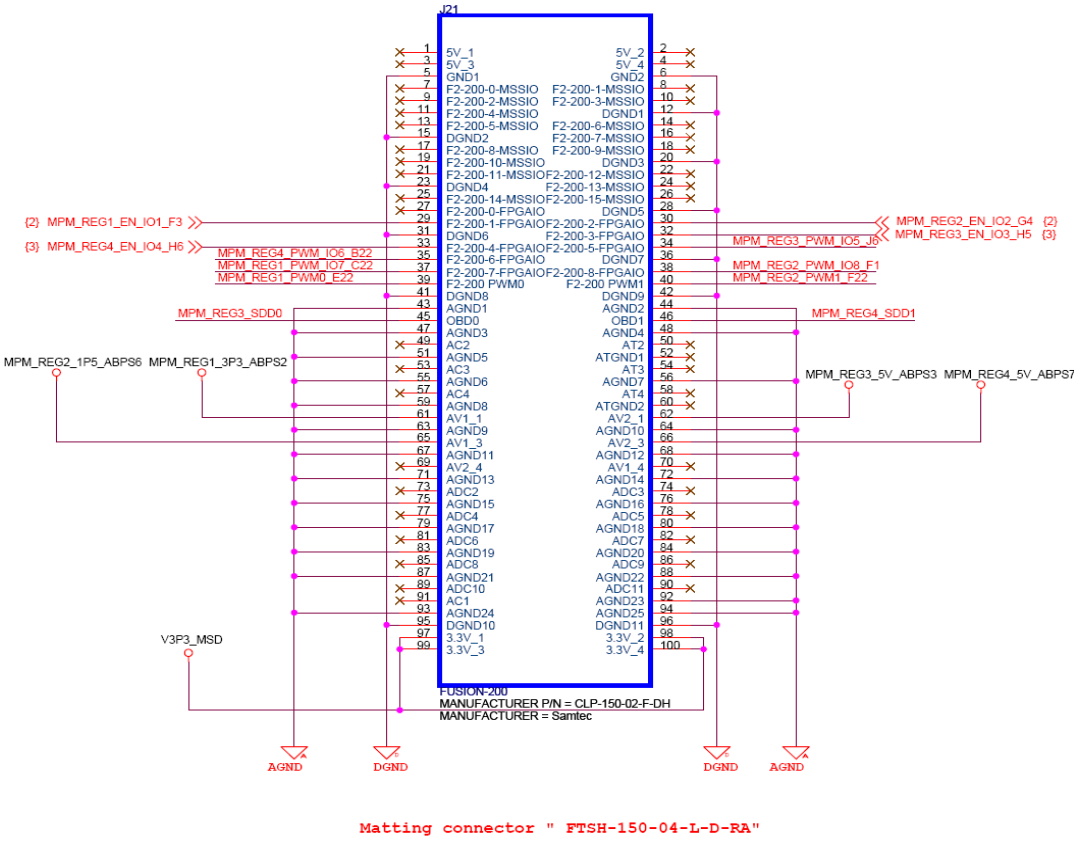

***Figure 3-7* • Mixed Signal Connector on MPM DB for Interface to SmartFusion Board**

Related Documents

SmartFusion Documents

www.actel.com/products/smartfusion/docs.aspx

Libero IDE Design Software

www.actel.com/products/software/libero/default.aspx

Appendix A - Manufacturing Information

MPM DB Board

Full PCB design layout is provided in the MPM Daughter Card Kit website. To view the PCB design layout files, you can use Allegro Free Physical Viewer, which can be downloaded from the Cadence Allegro Download page.

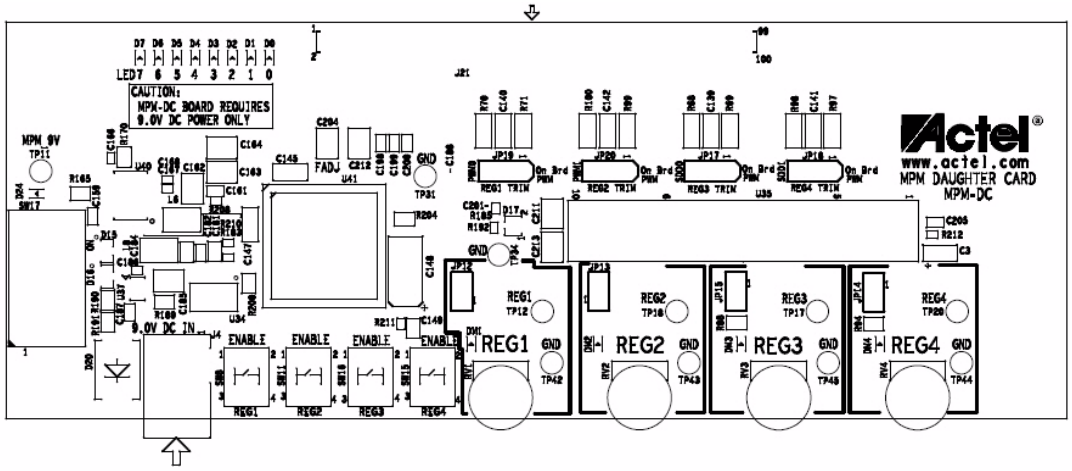

***Figure 3-8* • Top Silk Screen for MPM Daughter Board**

A – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found on the website at www.actel.com/company/contact/default.aspx.

Index

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