Power-Up/Down of Fusion FPGAs

Introduction

The Actel Fusion® Programmable System Chip (PSC) satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed-signal FPGA family, Fusion integrates configurable analog, Flash memory, and FPGA fabric in a monolithic PSC. Actel Fusion devices enable designers to quickly move from concept to completed design and deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Actel Flash-based FPGAs, including a high isolation, triple-well process and the ability to support high voltage transistors to meet the demanding requirements of mixed-signal system design.

As a Flash-based FPGA, a Fusion device is nonvolatile, offering a single-chip solution. Being live at power-up and capable of operating from a single 3.3 V power supply make Fusion an ideal system master for initiating, controlling, and monitoring multiple voltage supplies. An on-chip voltage regulator can be used to provide a 1.5 V power source to the FPGA fabric portion of Fusion and embedded Flash memory.

Glitches and brownouts in system power will not corrupt the Fusion device logic configuration. Fusion devices have no power-on surge, inrush current, or configuration current, as do SRAM-based FPGAs. Fusion devices offer additional power savings with both sleep and standby modes of operation.

Power Supply Requirements

Main power supplies for digital and analog components of Fusion devices are given in Table 1.

Table 1 • **Main Power Supplies of Fusion Devices**

Voltage	Power Supplies	Notes
1.5 V	Core Supply Voltage (V_{CC})	Supply voltage to the FPGA core, nominal 1.5 V. V_{CC} is also required for powering the JTAG state machine in addition to V_{JTAG}. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the Fusion device.
	Embedded Flash Power Supply (V_{CCNVM})	1.5 V power supply used by the Fusion device's Flash memory block module(s).
	PLL Supply Voltage ($V_{CCPLA/B}$)	Supply voltage to analog PLL, nominal 1.5 V. If unused, $V_{CCPLA/B}$ should be tied to GND.
	Analog Power Supply (V_{CC15A})	1.5 V clean analog power supply input for use by the ADC, AQ, and ACM.

Table 1 • **Main Power Supplies of Fusion Devices (Continued)**

Voltage	Power Supplies	Notes
3.3 V	I/O Supply Voltage (V_{CCI}Bx)	Supply voltage to the bank's I/O output buffers and I/O logic. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.
	JTAG Supply Voltage (V_{JTAG})	The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). If the JTAG interface is not used nor planned to be used, the V_{JTAG} pin together with the TRST pin could be tied to GND.
	Oscillator Power Supply (V_{CCOSC})	Power supply for both integrated RC oscillator and crystal oscillator circuit
	Analog Power Supply (V_{CC33A})	3.3 V clean analog power supply input for use by the ADC and RTC
	Negative 3.3 V Output (V_{CC33N})	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.
	Analog Power Supply ($V_{CC33PMP}$)	3.3 V clean analog power supply input for use by the analog charge pump.
	Programming Supply Voltage (V_{PUMP})	For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V.

Table 2 shows which power supplies are required for the operation of major functional blocks inside the Fusion device.

Table 2 • **Required Power Supplies for Operation of Fusion Blocks**

Fusion Blocks	3.3 V Supply Only	3.3 V and 1.5 V Supply
Fabric	OFF	ON
JTAG	OFF	ON
RCO/XTALOSC	ON	ON
I/O Banks	ON	ON
Embedded Flash memory (NVM)	OFF	ON
Real-time counter (RTC)	ON	ON
Analog to digital converter (ADC)	RESET STATE	ON
Analog Quad (AQ)	OFF	ON
Analog Configuration Multiplexer (ACM)	OFF	ON

Fusion devices can operate from a single 3.3 V supply by utilizing the Fusion integrated 1.5 V voltage regulator and an external pass transistor. The 1.5 V will drive the FPGA core and embedded Flash memory. The 1.5 V is not supplied to the device internally, but is routed on the board to the appropriate power supply pins on the Fusion device. This allows users the flexibility to either implement this power scheme or utilize other 1.5 V supplies that may already exist within their system.

Power-Up/Down Sequence and Transient Current

Fusion devices have no power-up or power-down sequencing requirements. To maximize power savings, Actel identifies three power conditions that will result in relatively high transient current:

1. When $V_{CC33PMP}$ is powered up before V_{CC33A}, there will be approximately 30 mA transient current on $V_{CC33PMP}$ until V_{CC33A} is powered up. In order to avoid this increase in current, Actel recommends that the 3.3 V supplies, V_{CC33A} and $V_{CC33PMP}$, be tied together.
2. Actel recommends tying V_{CCNVM} to V_{CC}.
   a. If V_{CCNVM} is powered up before V_{CC}, a static current of 30 mA (typical) may be measured on V_{CCNVM}.
      i. The current vanishes as soon as V_{CC} reaches V_{CCNVM} voltage level.
      ii. The same current is observed at power-down (V_{CC} before V_{CCNVM}).
   b. If V_{CC} is powered up before V_{CCNVM}, a static current of 30 mA (typical) may be measured on V_{CC}.
      i. The current vanishes as soon as V_{CCNVM} reaches V_{CC} voltage level.
      ii. The same current is observed at power-down (V_{CCNVM} before V_{CC}).
   c. If V_{CCNVM} is powered up simultaneously with V_{CC}, the maximum transient current on V_{CC} does not exceed the maximum standby current specified in the datasheet.
3. Actel recommends tying V_{CCPLX} to V_{CC} and using proper filtering circuits to decouple V_{CC} noise from the PLL
   a. If V_{CCPLX} is powered up before V_{CC}, a static current of up to 5 mA (typical) per PLL may be measured on V_{CCPLX}.
      i. The current vanishes as soon as V_{CC} reaches V_{CCPLX} voltage level.
      ii. The same current is observed at power-down (V_{CC} before V_{CCPLX}).
   b. If V_{CCPLX} is powered up simultaneously or after V_{CC}, the maximum transient current on V_{CC} does not exceed the maximum standby current specified in the datasheet.

In any other power-up/down sequence, no transient current is observed (i.e., the transient current during power-up remains less than the quiescent current of the Fusion device).

Digital I/O Behavior at Power-Up/Down

This section discusses the behavior of device I/Os, used and unused, during power-up/down of V_{CC} and V_{CCI}.

The voltage pins used for Fusion I/O activation are as follows:

- V_{CC}: Voltage supply to the FPGA core
- V_{CCI}Bx: Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number.

In Fusion devices, the JTAG I/O bank is powered separately and need only be powered when JTAG operations are desired. When implementing JTAG commands, both the FPGA core and the JTAG I/O bank must be powered.

I/O State During Power-Up/Down

During power-up of the Fusion device, all I/Os are in tristate mode. Only after both V_{CC} and V_{CCI} power supplies are powered up to their functional level are the I/Os configured to the desired user configuration (power supply functional levels are discussed in the "Power-Up to Functional Time" section on page 4). Similarly, during power-down, I/Os of each bank are tristated after the first power supply reaches its brownout deactivation voltage.

I/O State During Standby and Sleep Modes

During standby and sleep modes of operation, V_{CC} (1.5 V for the FPGA core) is off, V_{CC33A} (3.3 V supply to the voltage regulator) is on, and V_{CCI} (I/O power rails) is on or off. The state of each type of I/O is defined as follows:

- Analog inputs
  - Inputs are pulled-down to ground through a 1 M Ω resistor.
- Gate driver
  - Output is floating (or tristated). No extra current on V_{CC33A}.
- Digital inputs (with or without pull-up/down)
  - Inputs are tristated.
- Digital outputs
  - Outputs are tristated.
- Digital Bibufs (input/output)
  - Outputs and inputs are tristated.

Power-Up to Functional Time

At power-up, device I/Os exit the tristate mode and become functional when the last voltage supply in the power-up sequence (V_{CCI} or V_{CC}) reaches its functional activation level.

Fusion devices meet Level 0 live at power-up (LAPU); they can be functional prior to V_{CC} reaching the regulated voltage required. This important advantage distinguishes Fusion Flash devices from their SRAM-based counter parts. SRAM-based FPGAs, due to their volatile technology, require hundreds of milliseconds after power-up to configure the design bitstream before they become functional (Figure 1).

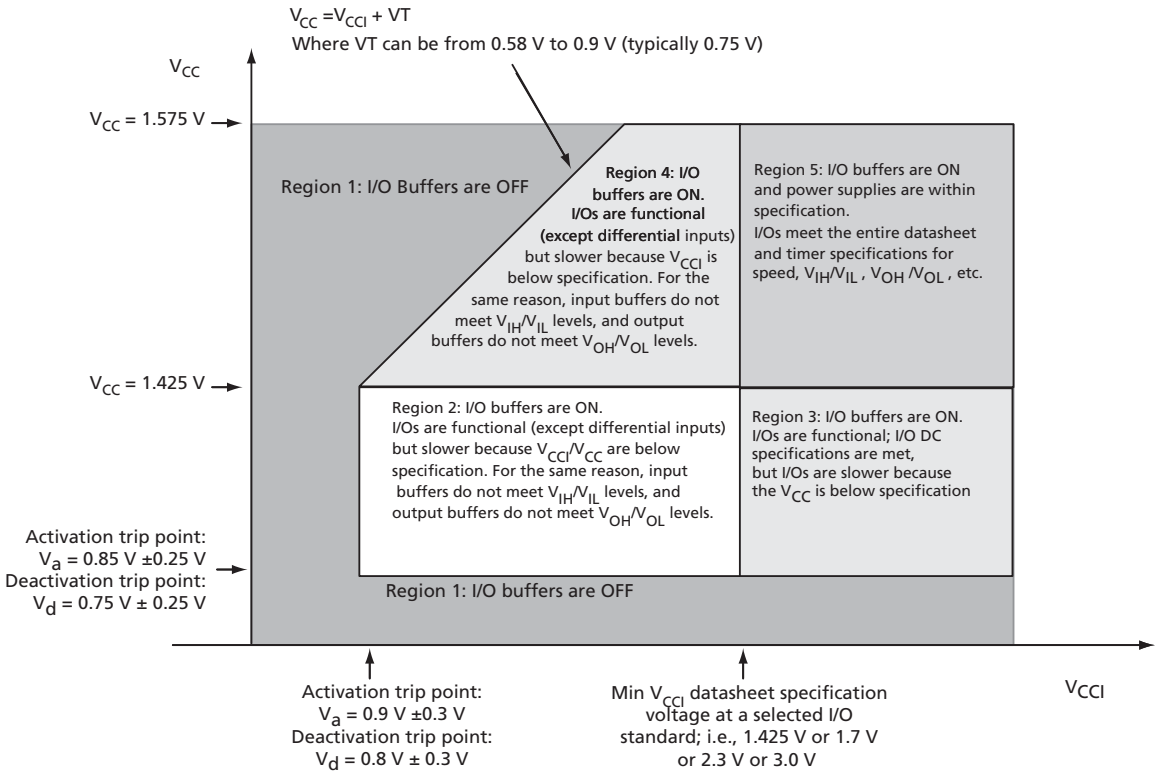

Figure 1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Brownout Voltage

Brownout is a condition in which the voltage supplies are lower than normal, causing the device to malfunction as a result of insufficient power. In general, Actel does not guarantee the functionality of the design inside Fusion devices if voltage supplies are below their minimum recommended operating condition. Actel has performed measurements to characterize the brownout levels of FPGA power supplies. The brownout levels of the power supplies for Fusion devices are designed to be 0.75 V+/–0.25 V for V_{CC} and 0.8 V+/–0.3 V for V_{CCI}. Characterization tests performed on two AFS600-PQ208E Rev A devices in typical operating conditions showed the brownout voltage levels to be within the specification.

PLL Behavior at Brownout Condition

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. The following sections explain PLL behavior during and after the brownout condition.

V_{CCPLx} and V_{CC} Tied Together

In this condition, both V_{CC} and V_{CCPLx} drop below the 0.75 V ± 0.25 V brownout level. During the brownout recovery, once V_{CCPLx} and V_{CC} reach the activation point (0.85 ± 0.25 V) again, the PLL output lock signal may still remain low with the PLL output clock signal toggling. If this condition occurs, there are two ways to recover the PLL output lock signal: 1) Recycle the power supplies of the PLL (power off and on) by using the PLL POWERDOWN signal; 2) Turn off the input reference clock to the PLL and then turn it back on.

Only V_{CCPLx} Is at Brownout

In this case, only V_{CCPLx} drops below the 0.75 V ± 0.25 V brownout level and the V_{CC} supply remains at nominal recommended operating voltage (1.5 V ± 0.075 V). In this condition, the PLL behavior after brownout recovery is similar to the initial power-up condition, and the PLL will regain lock automatically after V_{CCPLx} is ramped up above the activation level (0.85 ± 0.25 V). No intervention is necessary in this case.

Only V_{CC} Is at Brownout

In this condition, V_{CC} drops below the 0.75 V ± 0.25 V brownout level and V_{CCPLx} remains at nominal recommended operating voltage (1.5 V ± 0.075 V). During the brownout recovery, once V_{CC} reaches the activation point again (0.85 ± 0.25 V), the PLL output lock signal may still remain low with the PLL output clock signal toggling. If this condition occurs, there are two ways to recover the PLL output lock signal: 1) Recycle the power supplies of the PLL (power off and on) by using the PLL POWERDOWN signal; 2) Turn off the input reference clock to the PLL and then turn it back on.

It is important to note that Actel recommends using a monotonic power supply or voltage regulator to ensure proper power-up behavior.

Internal Pull-Up/Down

Fusion device I/Os are equipped with internal weak pull-up/down resistors that can be used by designers. If used, these internal pull-up/down resistors will be activated during power-up, once both V_{CC} and V_{CCI} are past their functional activation level. Similarly, during power-down these internal pull-up/down resistors will turn off when the first supply voltage falls below its brownout deactivation level.

Power-Up of Fusion FPGA Fabric Using Internal Voltage Regulator

The internal voltage regulator, when powered on, drives the FPGA core and embedded Flash memory, supplying all 1.5 V needs of the Fusion device.

1.5 V Voltage Regulator

In conjunction with an external pass transistor, the voltage regulator (VR) generates a 1.5 V power supply from the 3.3 V power supply (Figure 2). The VR can drive up to 20 mA of current to the base of the transistor. The maximum 1.5 V current supplied will depend upon the gain of the transistor utilized and the clamp current of the 3.3 V power supply. Using a typical transistor with a gain of 25, the 1.5 V output can easily supply current requirements for the Fusion device. If there are additional 1.5 V board requirements, the transistor can be sized accordingly. Actel recommends using the following transistors with the VR: PN2222A or 2N2222A.

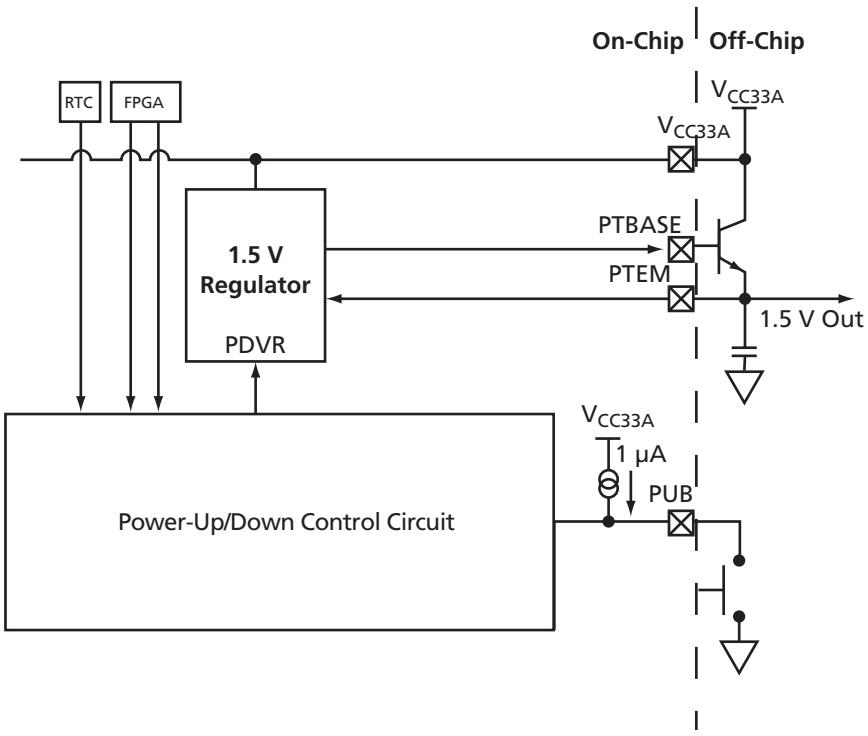

Figure 2 • **1.5 V Voltage Regulator (VR)**

Voltage Regulator and Power Supply Monitor

Since the functions of the voltage regulator logic and power system work together to control the power-up state of the FPGA core, these functions were combined into a single voltage regulator power supply monitor (VRPSM), as shown in Figure 3.

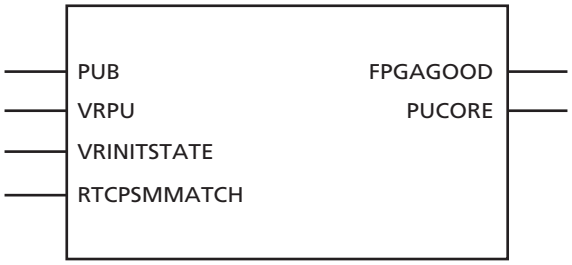

Figure 3 • **VRPSM Macro Block**

For more details on the components of the VRPSM, refer to Figure 5 on page 9.

The voltage regulator can be triggered by several signals: PUB, VRPU, MATCH signal from RTC or VRINITSTATE signal from the VR Init block.

The power-up bar (PUB) input comes from the PUB pin on the device, and hence can be a signal external to the Fusion device. The PUB is an active low input.

The VR Init block decides if the voltage regulator should turn on when the 3.3 V supply is first applied. Since the FPGA is not operating when the 3.3 V supply is off, the VR Init block lets the user define VR behavior at design time. When using the Actel SmartGen tool, the VRINITSTATE input of the VRPSM macro is configured. If turning on the VR at device power-up is desired, the VRINITSTATE is configured to logic 1.

The VRINITSTATE value is also the initial power-up value of the FPGAGOOD output signal of the VRPSM macro. This allows the user to drive FPGAGOOD to logic 1 or 0 even before the 3.3 V supply is up. When at logic 1 value, the FPGAGOOD signal indicates that the FPGA is logically functional. The default power-up value of FPGAGOOD is '0'. If at power-up, VRINITSTATE is '1' or the condition on VRPU, PUB, and RTCPSMMATCH triggers a VR power-up, then FPGAGOOD will be '1'. If VRPU, PUB, and RTCPSMMATCH are not driven, then FPGAGOOD is '0', unless it is already at '1'. In that case, it remains at '1'.

The PUB, VRPU, and RTCPSMMATCH values are never unknown. Pull-up logic for PUB and pull-down logic for VRPU ensure that PUB and VRPU are always at their default inactive values when they are not driven.

VRPU can not be driven to '1' before FPGAGOOD is '1'.

The VRINITSTATE input has equal priority with PUB, RTCPSMMATCH, or VRPU signals. For example, if at power-up both the VRINITSTATE and PUB signals are logic 0, the FPGAGOOD signal will be logic 1.

The PUCORE output is the PUB input inverted. The PUCORE output can be left floating. By connecting it to logic inside the fabric, it can be used as an indicator of the PUB pad status.

Power-Down of FPGA Fabric Using the Internal Voltage Regulator

Powering down the VR turns off the 1.5 V power supply to the FPGA fabric.

Once triggered, the voltage regulator remains on because of the latching functions of flip-flops. Only the FPGA fabric can reset these flip-flops and turn off the VR. Power-down of the VR is controlled by the input signal VRPU to the VRPSM macro. VRPU can be connected to internal logic in the FPGA fabric. Shown in Figure 5 on page 9, VRPU is also known as the FPGA_VRON signal.

Logic 1 on the VRPU input indicates that the VR should remain on, while logic 0 shuts off the regulator. A transition from logic 1 to logic 0 indicates an FPGA command to shut off the VR (and to shut off the FPGA if the FPGA is powered by the VR). The logic 0 state must be maintained until the FPGA shuts down in

order to complete the voltage regulator shutdown. However, if the PUB pad is held low, and hence active, the VR remains on regardless of the state of the VRPU signal.

JTAG Restriction to Powering-Off FPGA Fabric

The Fusion voltage regulator has been designed to be enabled whenever the JTAG port is active in order to make sure that the FPGA is powered-on during different JTAG operations (i.e., programming). The JTAG port is active when the TRST pin is at logic 1.

The TRST pin functions as an active low input to reset the boundary scan circuitry.

If the JTAG interface is active, the voltage regulator cannot be shut off regardless of the state of the VRPU signal. Hence, in order to turn off VR, the TRST pin must be grounded.

As already mentioned, by using the Actel SmartGen tool, the user can specify that the VR should be turned off at device power-up via VRINITSTATE signal. However, unless the TRST is grounded through a 470 Ω resistor, the VR will turn on as soon the board is powered up.

Periodic Power-Up/Down of FPGA Fabric

The Fusion real-time counter (RTC) system can be configured to power-up the FPGA fabric at a specific time or periodically. The RTC provides time-matching events that may be used so that whenever a match event occurs, the RTC controls power-up of the 1.5 V VR. After the FPGA fabric has completed its power-up sequence, its custom logic or soft microcontroller takes the appropriate actions, after which it controls the power-down of the voltage regulator, which turns the 1.5 V FPGA supply off.

Real-Time Counter (RTC)

The RTC operation requires a 3.3 V power supply, distinguishing it from the 1.5 V FPGA core and embedded Flash memory (Figure 4). The crystal oscillator must also be enabled in order to be used as a clock source for the RTC.

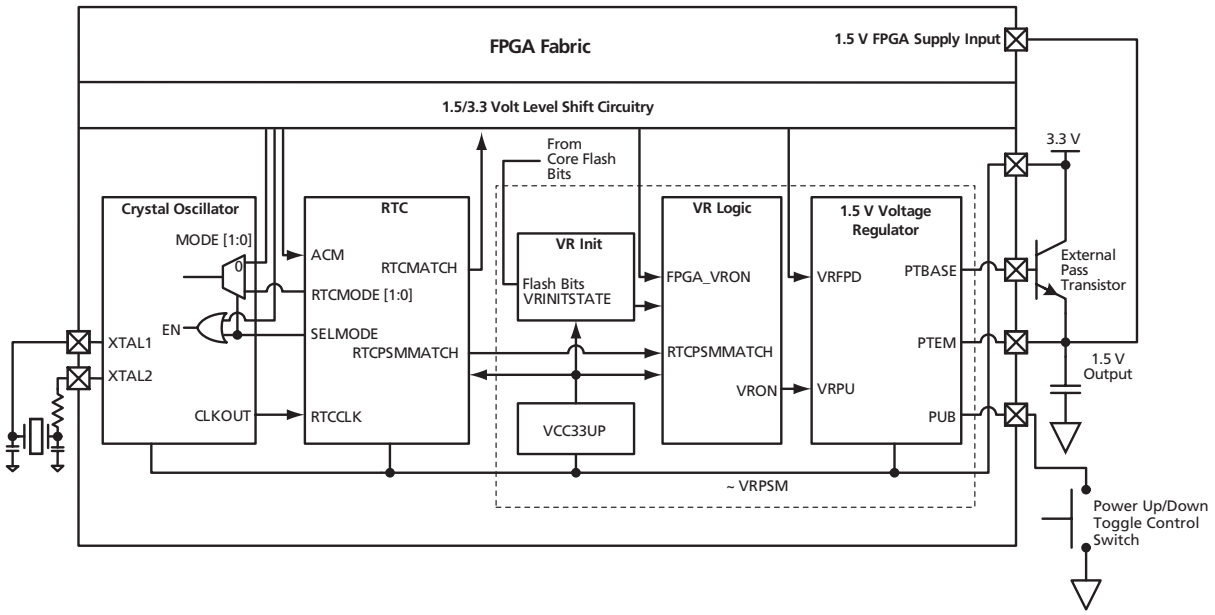

Figure 4 • **Real-Time Counter System**

The RTC, built from and controlled by a set of registers, is accessed via the analog configuration multiplexer (ACM). In Figure 5, a 40-bit loadable counter is used as the primary timekeeping element within the RTC. This counter can be configured to reset itself when a count value is reached that matches the value set within a 40-bit match register. As its reference clock, the counter logic uses a prescaled clock signal generated by the 7-bit prescaler block. Both the counter and match registers are addressable (read/write) from the FPGA and through a JTAG instruction.

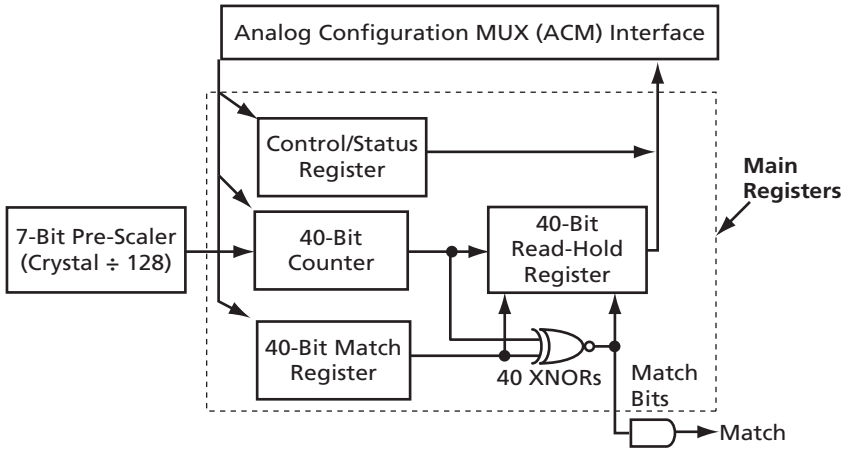

Figure 5 • **RTC Block Diagram**

When the device is first powered up (i.e., when the 3.3 V supply becomes valid), the 40-bit counter and 40-bit match register are cleared to logic 0. At this time, the MATCH output signal (provided by RTC) is active (logic 1). At any instance when the 40-bit counter value does not match the value in the 40-bit match register, the MATCH output signal will become inactive (logic 0).

The FPGA fabric portion of the Fusion device must be powered up and active at least once to write to the various registers within the RTC to initialize them for the user's application. Users set up the RTC by configuring the RTC from the Actel SmartGen tool, implementing custom logic, or programming a soft microcontroller.

The operation of the RTC is defined by the 8-bit control status register that is configured through ACM. For a periodic power-up/down of the VR using RTC, the following bits of the control status register must be set:

- The rtc_rst bit must be logic 0 so that the RTC reset is removed synchronously after 2 rising edges of ACM_CLK.
- The rstb_cnt bit must be logic 1 in order to allow the counter to count.
- The vr_en_mat bit must be logic 1 in order to enable the MATCH output port when a match occurs between the 40-bit register and the 40-bit match register.
- The rst_cnt_omat bit must be logic 1, allowing the counter to clear itself when a match occurs.
- The cntr_en bit must be logic 1, enabling the counter.

When using the Actel SmartGen tool to configure the RTC, the bits of the control status register are set by SmartGen. The user only needs to set these control bits when using a microcontroller.

During the power-down of the 1.5 V VR, the 3.3 V supply must remain active in order to keep the RTC actively counting for the next match event, which will cause a repeat power-up/power-down sequence to occur. In order to accomplish this, the match register must be set to the period of time that will be repeated for the power-up/power-down sequence.

Basic Operation Modes

The addition of the RTC system enables Fusion devices to support both standby and sleep modes of operation.

Standby

In standby mode with the 3.3 V power supply applied, the FPGA is not powered on. The crystal oscillator is turned on and the RTC is running off the 3.3 V input to the Fusion device. Furthermore, the 1.5 V voltage regulator is off. The voltage regulator can be turned on by reaching a match count in the RTC or by grounding the PUB pad.

Sleep

With the 3.3 V power supply applied, the FPGA is powered off in the sleep operation mode. The crystal oscillator, RTC, and VR are all turned off. The voltage regulator can be turned on by an external stimulus (i.e., push button) applied to the PUB pin.

It takes 100 µs for the voltage regulator to re-power if PUB pin is not driven to '0' when JTAG comes out of the reset. In order to avoid this power-up delay, PUB should be driven to '0' when TRST changes from '0' to '1'.

Conclusion

Fusion family devices are live at power-up and do not suffer from high the inrush and configuration currents associated with SRAM technologies. Fusion offers further power savings with standby and sleep modes of operation. Utilizing the integrated 1.5 V voltage regulator, Fusion devices can operate from a single 3.3 V power supply, thereby eliminating the need for any power supply sequencing, making Fusion an ideal system master.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (51900150-1/4.08*)	Page
51900150-0/7.06	In Table 1, Quiet I/O Supply Voltage (VMVx) was deleted.	1
	The two conditions in the "Power-Up/Down Sequence and Transient Current" section were updated and condition 3 is new.	3
	The "PLL Behavior at Brownout Condition" section and all its subsections are new.	5
	V_{CCPLL} was changed to V_{CCPLX}.	N/A

Note: **The part number is located on the last page of the document.*

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655
USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Room 2107, China Resources Building
26 Harbour Road
Wanchai, Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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